Reed Electronics Group

# EDN®

VOICE OF THE ENGINEER

DEC 1

Issue 25/2006

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## CREATING THE POWER SUBSYSTEM IN MODERN DESIGN

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POWER

FROM LINEAR TO DIGITAL

## PROPRIETARY ARCHITECTURES DEFEND AUTOMOTIVE SEGMENT

Page 47

## BATTLING BUGS Page 79

## EMBEDDED MEMORY EVOLVES

Page 89

# Ultimate Precision. Low Power. Small Size.

## Amplifiers Use TI's New 36V Bipolar SiGe Process

| Device | Input | $V_N$ | $V_{OS}$ | GBW | $I_Q$ | $V_S$ | Package |
|---|---|---|---|---|---|---|---|
| OPA211 | Bipolar | 1nV/√Hz | 100µV | 80MHz | 3.5mA | ±18V | MSOP-8 |
| OPA827 | JFET | 4.5nV/√Hz | 250µV | 18MHz | 4.2mA | ±18V | MSOP-8 |

The new OPA211 and OPA827 precision amplifiers from Texas Instruments offer lower power, smaller package size and lower noise, enabling breakthrough performance in test and measurement, instrumentation, imaging, medical, audio and industrial process control applications. The amplifiers were developed using the industry's first complementary bipolar 36V SiGe process, BiCom3HV.

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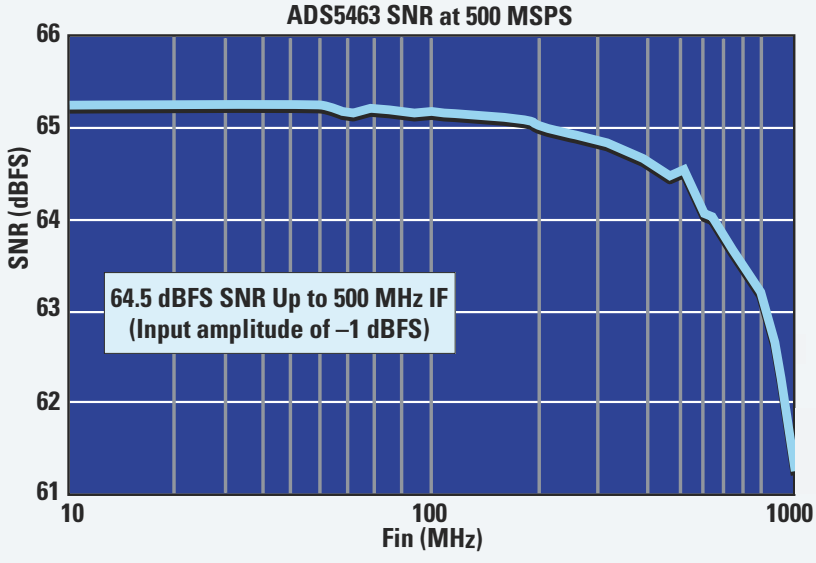
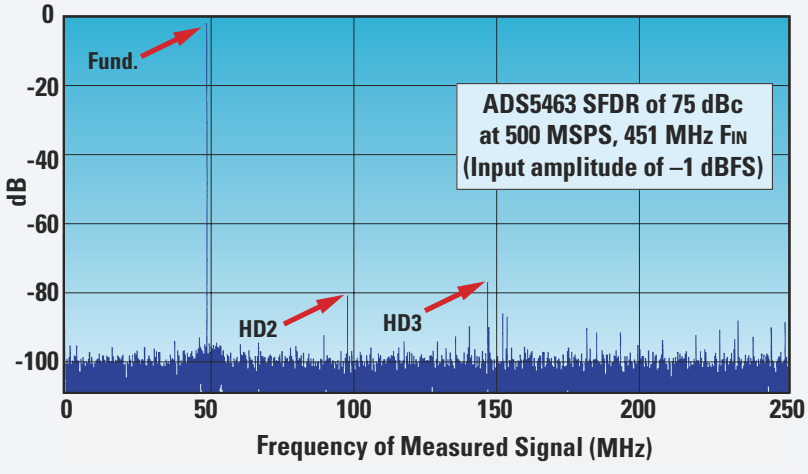
DATA CONVERTERS

# 12-Bit, 500 MSPS ADC




## ▶ Applications

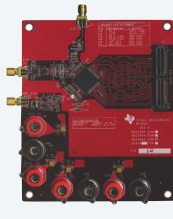
- Power amplifier linearization
- Multi-carrier receivers
- Software defined radio
- Radar and advanced imaging
- Test and measurement

## ▶ Features

- 12-bit resolution, 10.5 ENOB
- 2 GHz input bandwidth
- Space saving package size: 80-pin TQFP (14mm x 14mm)
- Differential input: 2.2 $V_{PP}$
- LVDS outputs with simplified data capture
- Total power dissipation: 2.25W
- Ind. temp: ADS5463 –40° C to +85° C
- Mil. temp: ADS5463-EP, QMLV –55° C to +125° C
- Pin-compatible with 13-bit, 210 MSPS ADS5440 and 13-bit, 250 MSPS ADS5444
- Recommended amplifiers: THS9000, THS9001, THS4304, THS4509, THS4511
- In production now: Priced at $125 in 1k units (Industrial temp. only)

The 12-bit, 500 MSPS **ADS5463** from Texas Instruments delivers best-in-class performance with greater than 75 dBc SFDR and 64.5 dBFS SNR for input frequencies through 450MHz. This new ADC benefits the most demanding amplifier linearization, communications, radar, imaging, test and measurement applications – all in a 14mm x 14mm 80-pin TQFP package. The ADS5463 is part of a pin-compatible family of products that include TI's 13-bit 250/210MSPS ADS5444 and ADS5440 ADCs.

For Evaluation Modules, Samples and Technical Information



**www.ti.com/ads5463 ○ 800.477.8924, ext. 13476**

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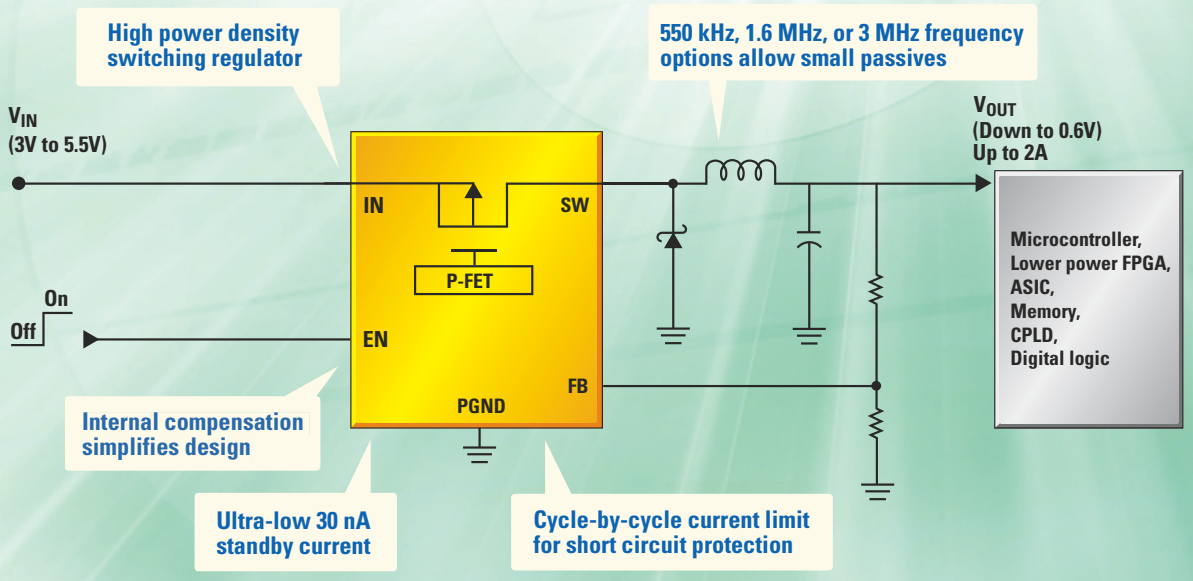
# High Power Density Switching Regulators Deliver Up to 2A Output Current

## Tiny LM2830/31/32 Step-Down Regulators Minimize External Components and Shrink Footprint

**System Power Configuration**

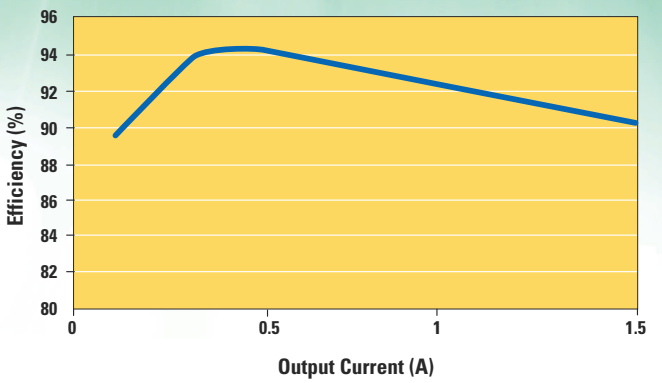



| Product ID | $I_{OUT}$ | Packaging |
|---|---|---|
| LM2830 | 1A | SOT23-5, LLP-6 |
| LM2831 | 1.5A | SOT23-5, LLP-6 |
| LM2832 | 2A | eMSOP-8, LLP-6 |

AVAILABLE LEAD-FREE

Ideal for use in multimedia set-top boxes, USB–powered devices, DSL modems, and hard disk drives

**LM2831 Efficiency vs Output Current**





**For FREE samples, datasheets, online design tools, and more information on the LM2830/31/32, contact us today at:**

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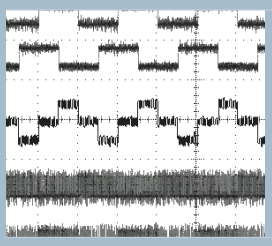
12.1.06

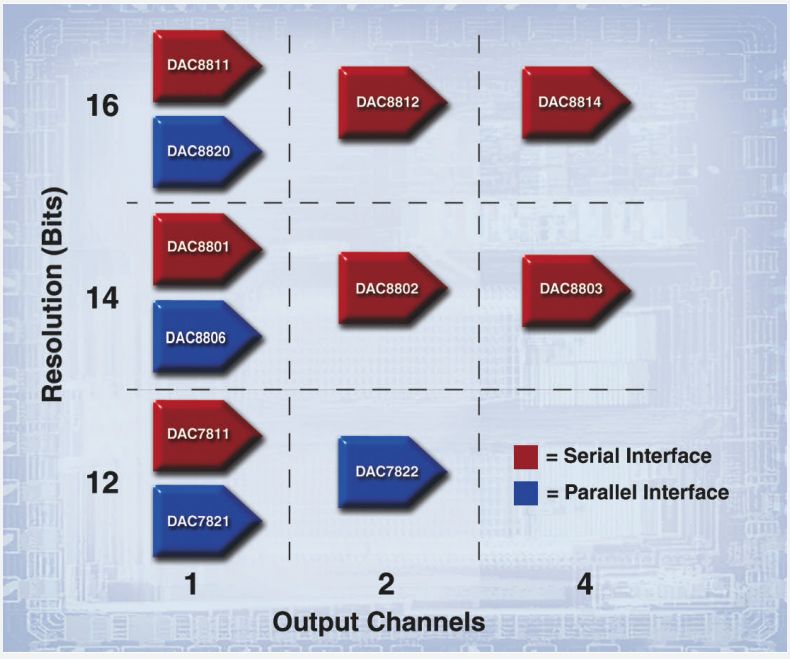


# DESIGNIDEAS



# Upgrade Your DAC Designs

## Multiplying D/A Converter Family




Burr-Brown Products from Texas Instruments

### ▶ Applications

- Automated test equipment
- Instrumentation
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- Industrial control
- Optical networking

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- Pricing in 1k units (starts at):
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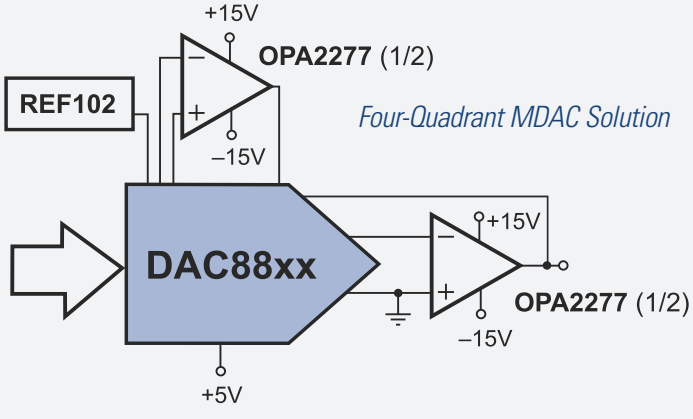
  - 14-bit: $4.60
  - 16-bit: $7.15

The **DAC88xx** and **DAC78xx** four-quadrant multiplying DACs from Texas Instruments feature high accuracy, low power and a variety of resolution and channel count options. Available in industry-standard pin configurations, the devices enable easy design upgrades based on speed, power and precision requirements. Simplify the selection of your output amplifier with TI's *MDACBufferPro* interactive selection tool.




*Four-Quadrant MDAC Solution*

**NEW!**
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Datasheets, Samples and *MDACBufferPro* Software

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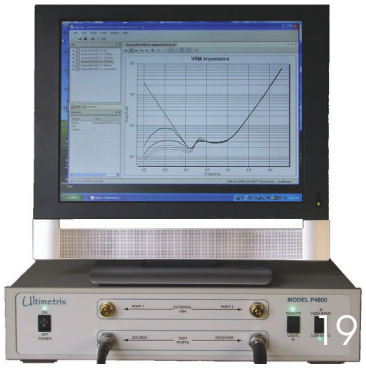
# contents 12.1.06

## pulse

Dilbert 20





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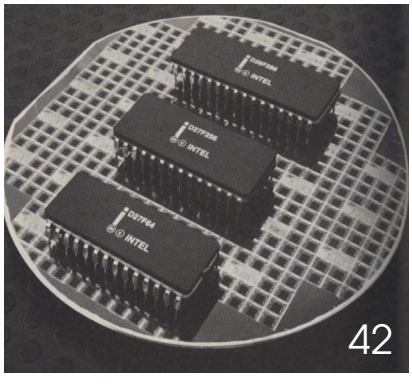

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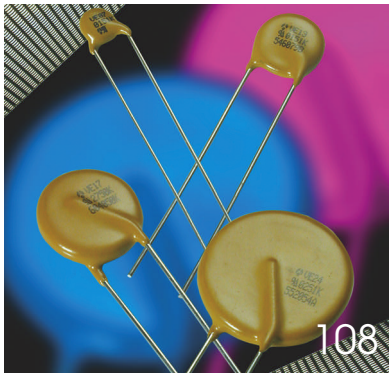

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## DEPARTMENTS & COLUMNS



## PRODUCT ROUNDUP




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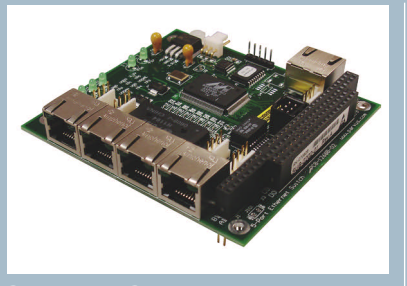

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**Ciranova tool finds way around Cadence SKILL for analog design**
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## AUDIOCASTS

The globalization of design: A conversation with Harley Feldberg, Avnet Electronics Marketing

→ www.edn.com/article/CA6390243

Microcontroller and embedded networks: A conversation with Microchip Chief Executive Officer Steve Sanghi

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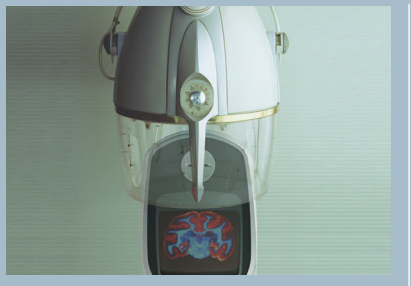

## READERS' CHOICE

*A selection of recent articles receiving high traffic on www.edn.com.*

**Mobile makeover: Hijack a smart-phone interface for embedded-systems control**
→ www.edn.com/article/CA6382645

**Embedded-processing platforms: a second look**
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**LED senses and displays ambient-light intensity**
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**Lab publicizes another Wi-Fi worry**
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**High-speed bus for PC management emerges**
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**Single microcontroller pin senses ambient light, controls illumination**
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**It's not too late** to nominate your company's engineers and products for the 17th Annual *EDN* Innovation Awards. We've extended the nomination deadline to December 8. Our online process makes it easy. The awards ceremony will take place April 2, 2007.
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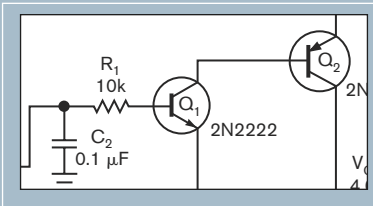


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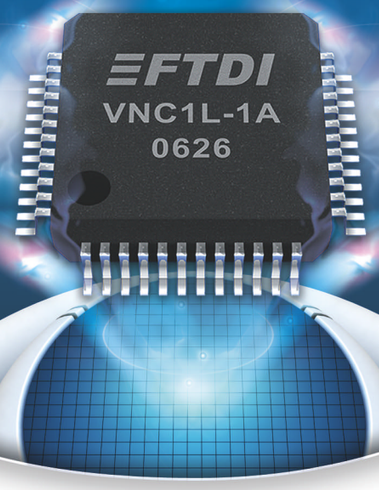
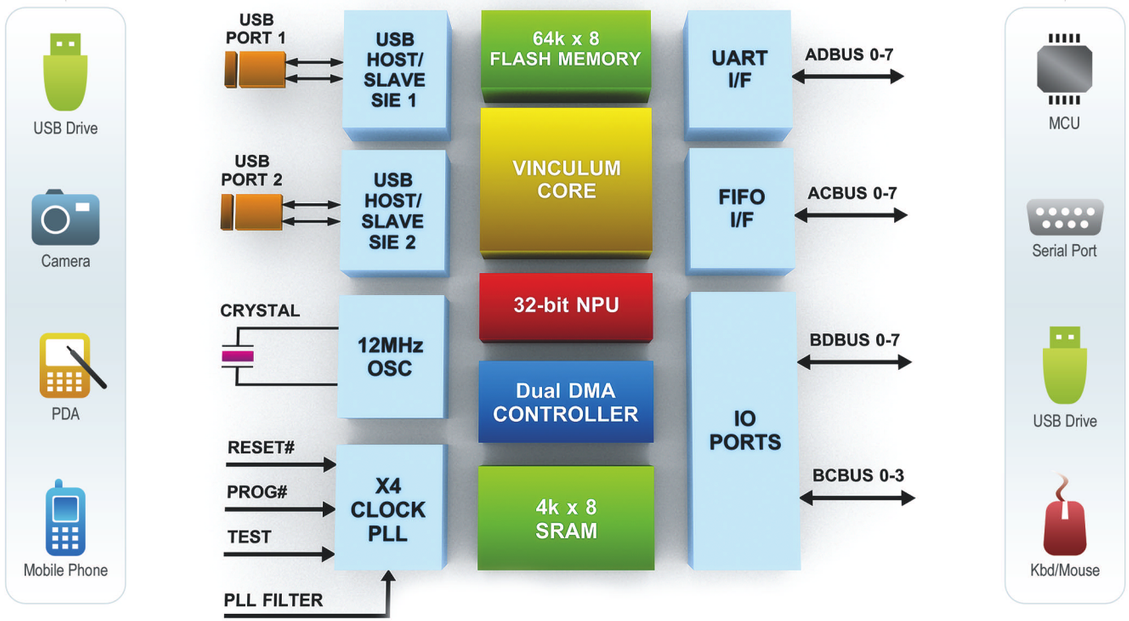
# FIRE YOUR IMAGINATION



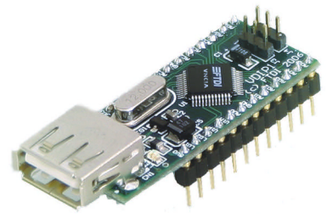

VINCULUM
BINDING USB TECHNOLOGIES

FTDI Chip

The **Vinculum** family of USB Host Controller not only handles the USB Host interface and data transfer functions, but owing to the inbuilt processor core and embedded Flash memory, Vinculum encapsulates the USB device classes as well. When interfacing to mass storage devices such as USB Flash drive, digital camera, or PDA, Vinculum also transparently handles the FAT File structure communicating via UART, SPI or parallel FIFO interfaces via a simple to implement command set. Vinculum provides a new cost effective solution for providing USB Host capability into products that previously did not have the hardware resources available.

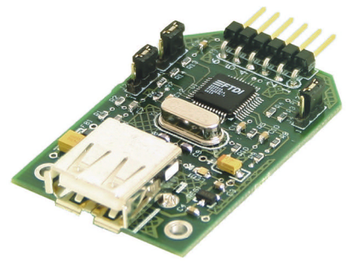



## Vinculum Evaluation Modules & Application Areas



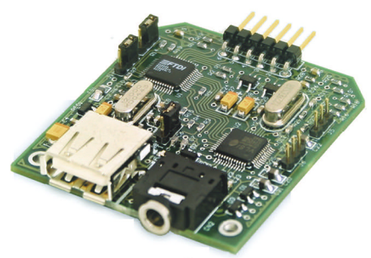
The **VDIP1** module is an MCU to USB Host Controller development module for the VNC1L device and is ideal for rapid prototyping and development of VNC1L designs.

- Jumper selectable UART, SPI or FIFO MCU Interfaces
- USB "A" type socket to interface with USB peripherals
- 2nd USB Interface available via module pins if required
- Single 5V supply input
- Auxiliary 3.3V/200mA power output to power external logic
- Traffic Indicator LEDs



**VDRIVE1** is possibly the easiest solution for adding a USB Flash Drive interface to existing products. Only four signal lines plus 5V/GND are required to be connected.

- One USB "A" socket to connect to USB Flash Drive
- Link Selectable UART or SPI interface
- Only 4 signals to connect excluding PWR/GND
- Single 5V supply required
- Easy to implement command set



**VMUSIC1** is a product that not only lets you add USB Flash Drive interfacing to your product but allows you to play back MP3 and other popular digital music formats direct from a USB Flash Drive.

- One USB "A" socket to connect to USB Flash Drive
- Stereo 3.5mm headphone jack socket and audio line-out connector for audio playback.
- Link Selectable UART or SPI interface
- Only 4 signals to connect excluding PWR/GND
- Single 5V supply required
- Easy to implement command set

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BY MAURY WRIGHT, EDITOR IN CHIEF

# CEOs spotlight chip-maker challenges to innovation

On opening day at Electronica 2006 (Munich, Germany), a CEO panel on innovation kicked off the festivities at the megaconference. Moderator Hermann Simon, chairman of Simon-Kucher & Partners, quizzed the participants—Frans van Houten of NXP, Satoru Ito of Renesas, Michael Mayer of Freescale, and Wolfgang Ziebart of Infineon—on the challenges that the IC makers face as they strive to innovate and prosper. Attendees at the 90-minute event heard more boasts about financial results and leadership positions than compelling insight into today's challenges. But I did find a couple of tidbits among the hype.

Actually, the panel got off to a rough, or at least a slow, start, because the CEOs were presenting what I felt were well-understood facts. The foursome spent too much time acknowledging that the consumer market—specifically, digital-media products—was the new tech-industry driver. Still, I was a bit surprised to hear the extent to which consumer was dominating in IC shipments. Ziebart of Infineon revealed that the volume of ICs that the company sells into consumer products today exceeds the volume sold into the IT and government markets combined.

Mayer of Freescale was quick to note that selling into what he termed the embedded market was also far different from selling into the IT or PC markets. He pointed out that in applications from cars to the modern toaster, the chip designers must know far more about the end application than ever before. We at *EDN* have certainly witnessed that trend for years, and it's guided our efforts to regularly present application articles. And the CEOs confirmed what we've been hearing about IC companies hiring more and more software developers to address the application challenge.

**The discussion turned to how fast the companies must move to develop new technology that might allow them to capture future opportunities.**

The most thought-provoking insights came from NXP's van Houten. He pointed out the differences in the timing challenge that IC and end-product makers face. The end-product companies work on nine- to 18-month development cycles. To be competitive with escalating consumer demands requires that churn rate. And the end-product makers can meet such demand only because the IC makers these days take on so much of the product design. But, as van Houten pointed out, IC makers are working on three- to five-year cycles in process-technology road maps while also carrying a bigger chunk of the end-product responsibility. Perhaps there is nothing astounding in these thoughts, but I hadn't considered the challenge to the IC maker in quite that way before.

Quickly, the discussion turned to how fast the companies must move to develop new technology that might allow them to capture future opportunities. Ziebart of Infineon stressed "right timing" over speed and decried "innovation for innovation's sake." Simon asked whether perhaps an emphasis on moving to new technologies too fast might be behind Sony's recent troubles in notebook batteries and the PlayStation 3. The panel members were unwilling to directly address Sony's plight but conceded that moving too early could put an IC company in a bind.

Van Houten of NXP was most bullish on pushing fast in moving to new technologies. He related the oft-heard claim from IC makers about being in first or second market position in key markets. But he backed that boast with a dig at companies that move timidly. He also related that companies that move more slowly and win a position such as fourth, fifth, or sixth when it comes to market share still ultimately spend the same R&D dollars as the first movers and don't achieve the return on investment. Even Renesas' Ito stated, "Speed is necessary to serve the consumer market."

Finally, the group talked a bit about the future. NXP's van Houten again stood out, noting that advancements similar to those happening in the consumer market would come to segments such as health care or nonentertainment segments, such as lighting. He claimed, for instance, that solid-state lighting would replace existing incandescent and fluorescent lighting much more quickly that most people believe—clearly defining what he believes to be another opportunity. EDN

*Contact me at mgwright@edn.com.*

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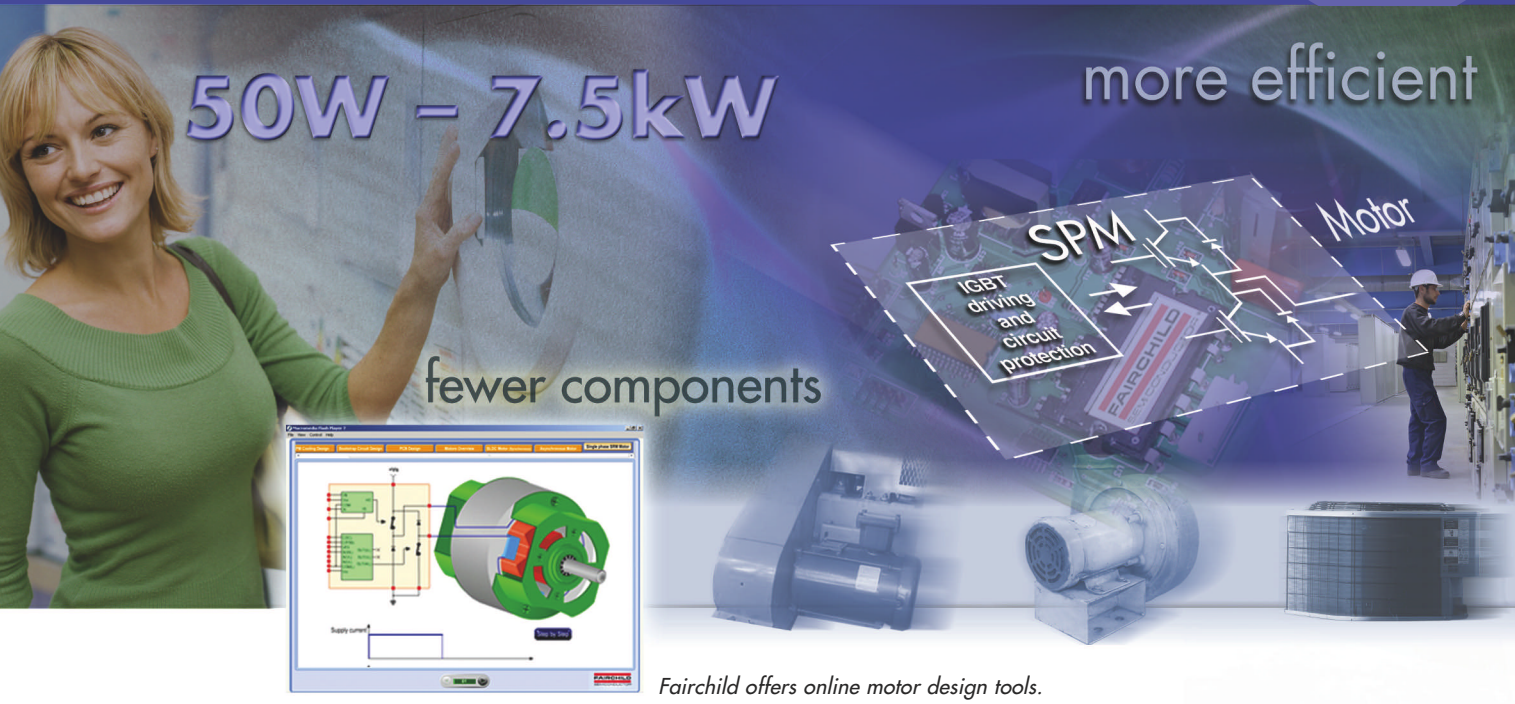


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| SPM Series | Motor Ratings | Description |
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| PFC-SPM | 1kW to 3kW | Partial switching converter module |
| | 3kW to 6kW | Power Factor Correction (PFC) module |

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///12653//>8//**--{{}}:)
88/483//[8840]//::(000121)/--
065=0U812:/-*--38}/////093200
8/{88498}/-**//9938500{099}87
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088903-3868**0//59030{59840}998
8350//5929*548**W8399/238493//30
[7950983/*::5638(5530)5849]58300//54
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(779:<348){**/})84030/84890//R42{RUN}
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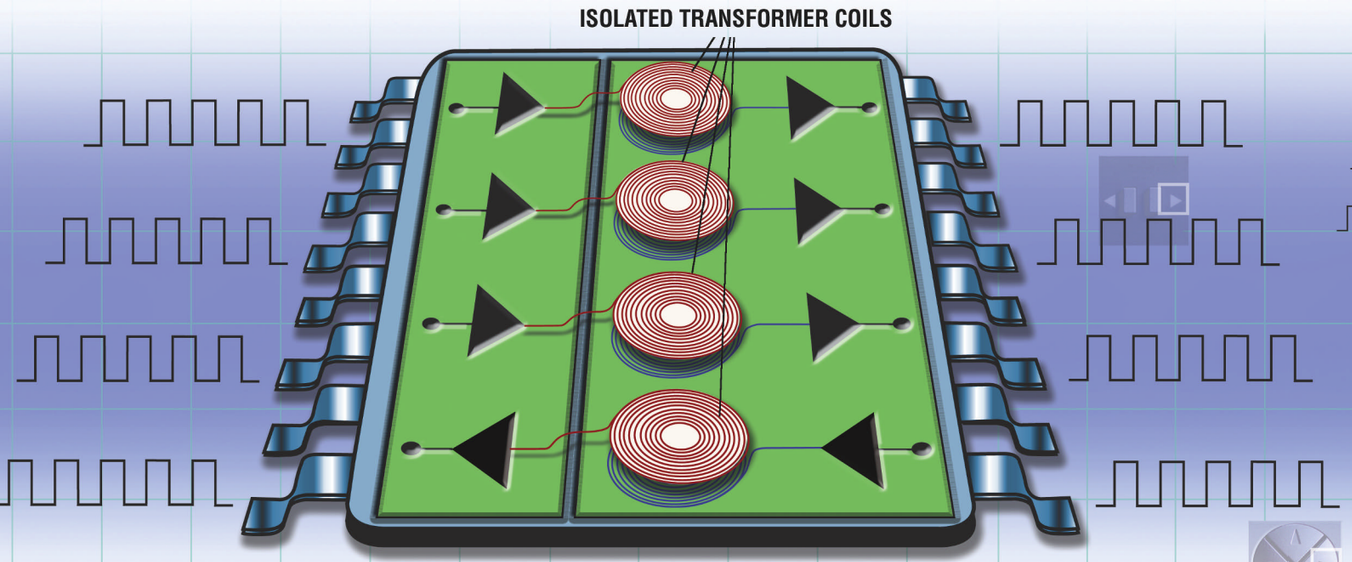


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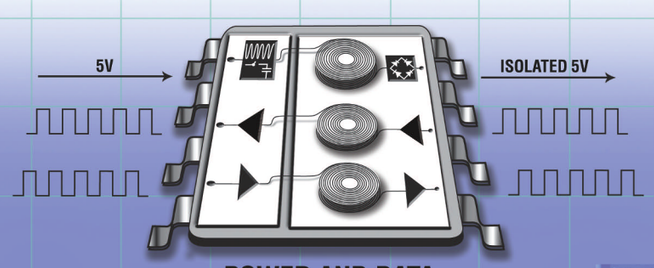
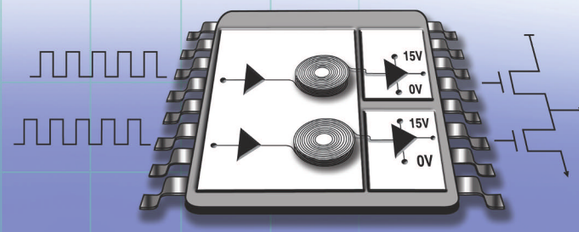



## POWER AND DATA

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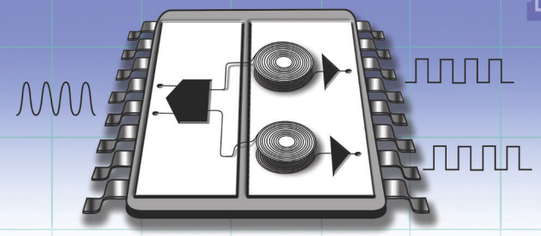

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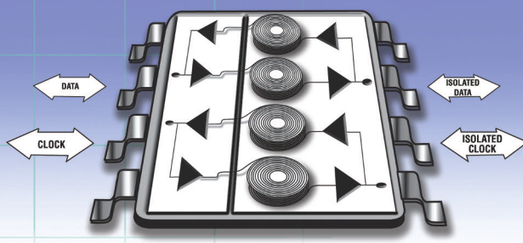


## COMMUNICATIONS

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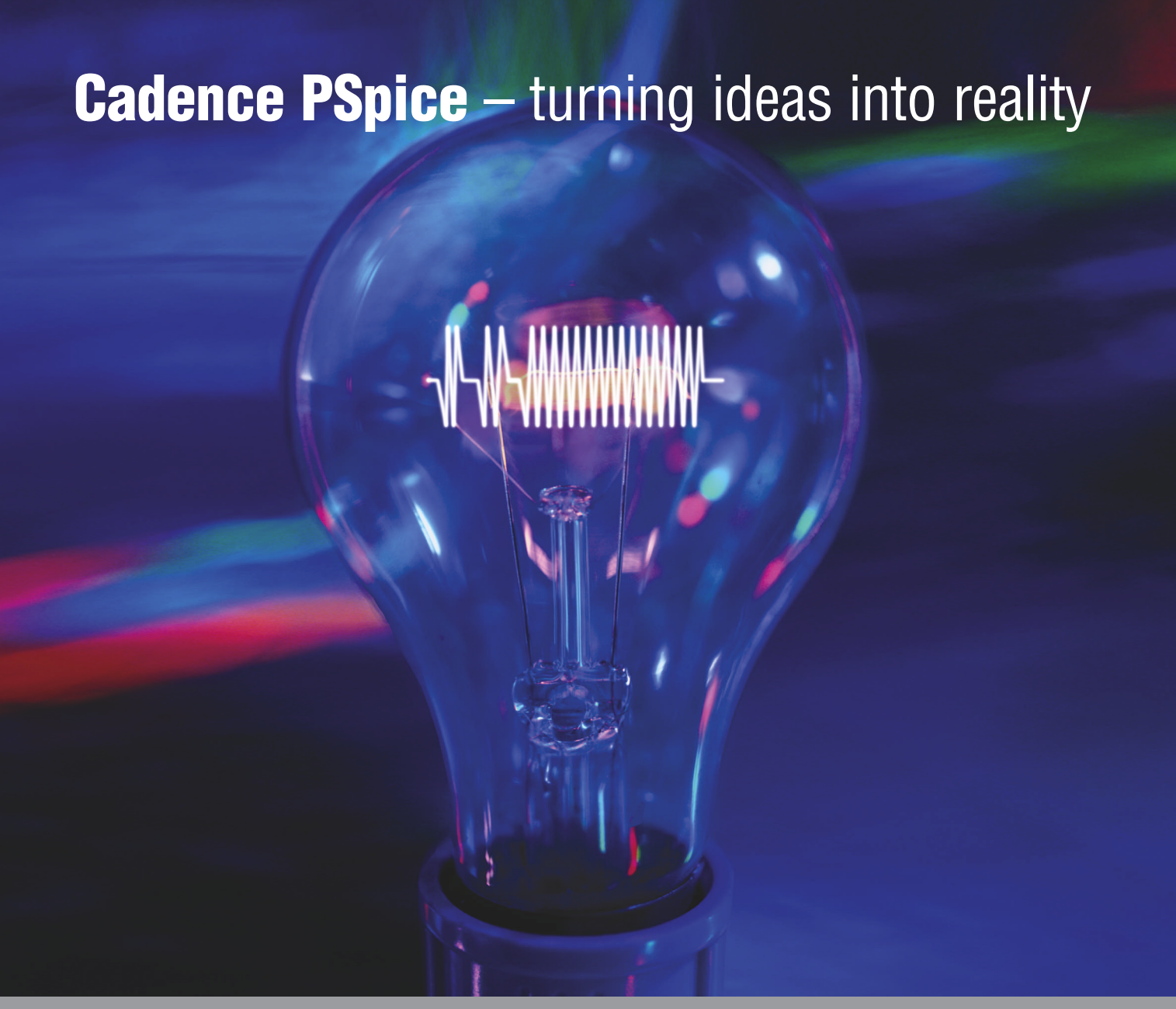
ANALOG DEVICES

# **Cadence PSpice** – turning ideas into reality



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# pulse

INNOVATIONS & INNOVATORS

## Power-delivery network analyzer measures 50-μΩ impedance

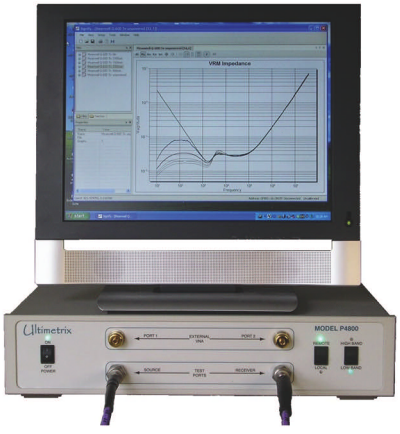
The Ultimetrix P4800 PDNA (power-delivery network analyzer) measures impedances as low as 50 μΩ from 10 Hz to 40 MHz as a stand-alone instrument or to 18 GHz when you interface it to an external vector-network analyzer. This capability allows impedance measurement of devices under test in a continuous sweep across more than nine decades of frequency. The methodology uses a four-point Kelvin technique, which, besides providing high accuracy and sensitivity, is immune to errors caused by contact resistance and inductance.

The instrument's primary application is in characterizing power-delivery networks on pc boards and in IC packages and for characterizing network components, such as decoupling capacitors and voltage-regulator modules. The analyzer allows you to test devices ranging from individual components to fully populated, live system boards.

According to Ultimetrix, the product addresses a growing need for lower impedance power-delivery networks, which results from the use of ICs that require increased supply current at lower voltages. The Ultimetrix P4800 PDNA, including software, cabling, and a year of application support, costs approximately $46,500. For a more complete description, go to www.edn.com/061201p1.

**—by Dan Strassberg**

▷**Ultimetrix Inc**, www.ultimetrixinc.com.




The P4800 PDNA measures impedances as low as 50 μΩ from 10 Hz to 40 MHz as a stand-alone instrument or to 18 GHz when interfaced to an external vector-network analyzer.

### FROM THE VAULT

**"Not too long ago, we reached an important milestone; the value of software in electronic products outstripped the value of the hardware. ... Many companies and managers treat software as if it were a poor relation. It becomes easy to say, 'It's only a few lines of code. What could go wrong?'"**

—Jon Titus, Editor, *EDN*, Sept 2, 1991

## Mixed-signal-SOC designs get flash for auto and industrial applications

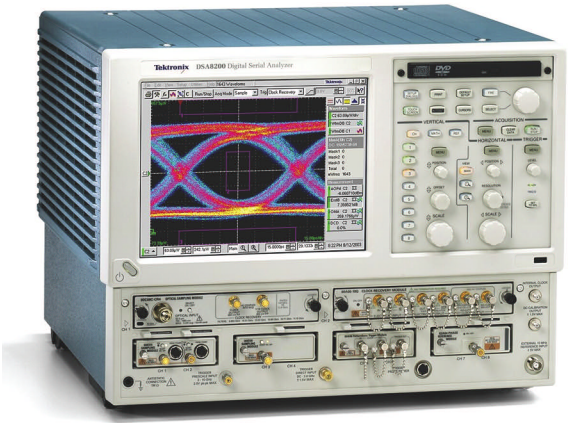
The term "SOC" (system on chip) typically conjures thoughts of the incredibly dense digital IC that lies at the heart of a consumer-electronics product, but designers targeting auto, industrial, and similar applications need SOCs, as well. However, these applications demand complex analog functions and tolerance of high-voltage environments. AMI Semiconductor targets such needs with its 0.35-micron Smart Power SOC process for custom-IC and structured-ASIC designs, and now designers can add flash memory to such designs.

AMI introduced the HiMOS (high-injection-MOS) IP (intellectual property) at Electronica, which took place last month in Munich, Germany. The process technology retains stored data for 15 years in harsh environments and supports operation to 80V over a −40 to +120°C temperature range. Designers can now add as much as 64 kbytes of flash to SOC designs that can also include data converters and interfaces, such as CAN (controller-area network) and LIN (local-interconnect network).**—by Maury Wright**

▷**AMI Semiconductor**, www.amis.com.

# Sequential-sampling scopes, TDR challenge VNAs

Tektronix has announced the DSA8200 digital-serial-analyzer sequential-sampling oscilloscope, new remote-sampling electrical modules, and enhanced IConnect software for serial-data-network analysis. According to the company, the TDR (time-domain-reflectometry) and electrical modules represent the most significant performance advancement in TDR-test technology in 20 years—a direct response to the demanding needs and compliance requirements of high-speed serial-data standards.



According to the manufacturer, quicker setup and measurements will enable high-performance sequential-sampling scopes, such as the DSA8200, along with new TDR modules and iConnect software, to displace VNAs in serial-data-network analysis, despite VNAs' edge in dynamic range and accuracy.

The emergence of multigigabit-serial standards is driving down power budgets and timing margins. As a result, accurate analysis of signal paths and interconnects in both the time and the frequency domains is critical to a full understanding of the effects of loss and crosstalk. Industry standards, such as PCI Express, Serial ATA (advanced-technology attachment), XAUI (10-Gbps attachment-unit interface), and InfiniBand, increasingly call for the use of S (scattering) parameters and impedance measurements to characterize the effects and ensure system interoperability. "With a 2.5-times increase in TDR performance and new automation tools, the new DSA8200 perfectly matches serial-data-network-analysis requirements," says a Tek spokesperson. "The DSA8200 represents the highest performance and most cost-effective approach to accurate and repeatable S-parameter measurements at the 1- to 12.5-Gbps serial-data rates of current and emerging differential standards."

> The modules include such usability features as channel-to-channel and module-to-module deskew of ±250 psec.

The primary alternative to TDR has been the VNA (vector-network analyzer), a specialized, dedicated frequency-domain instrument. However, the VNA requires extensive setup and calibration routines and can be significantly more expensive than a high-performance TDR. S-parameter-measurement routines for serial-data-network analysis that often require hours to set up and execute using a VNA usually take just a few minutes using TDR. Moreover, TDRs' higher noise floor and lower resolution are usually adequate for serial-data-network analysis.

Four new electrical modules feature high bandwidth and low noise. The modules include such usability features as channel-to-channel and module-to-module deskew of ±250 psec, user-selectable bandwidth, and small-form-factor remote samplers. Each channel has a fully integrated 2m cable with a remote sampler that brings the TDR head close to the device under test, minimizing the effects of probes, cables, and fixtures and ensuring the highest possible system fidelity for measurement accuracy and repeatability. The 80E10 dual-channel true-differential TDR module provides a 12-psec incident and 15-psec reflected TDR rise time, 50-GHz bandwidth, and 600-μV-rms noise, which is the lowest noise at this performance level, according to Tek. The devices also feature independent step generation for true-differential measurements.

Other modules include the 80E08, a dual-channel TDR electrical module with 18-psec incident and 20-psec reflected rise times, and 300-μV-rms noise at 30-GHz bandwidth. Two new dual-channel, low-noise electrical modules, the 80E09 and 80E07e, feature 450-μV-rms noise at 60 GHz and 300-μV-rms noise at 30 GHz, respectively. US list prices for the DSA8200 mainframe begin at $20,900. Prices for TDR modules, sampling modules, and iConnect software packages start at $27,100, $22,000, and $7900, respectively.**—by Dan Strassberg**

▷**Tektronix Inc**, www.tek.com.

DILBERT By Scott Adams

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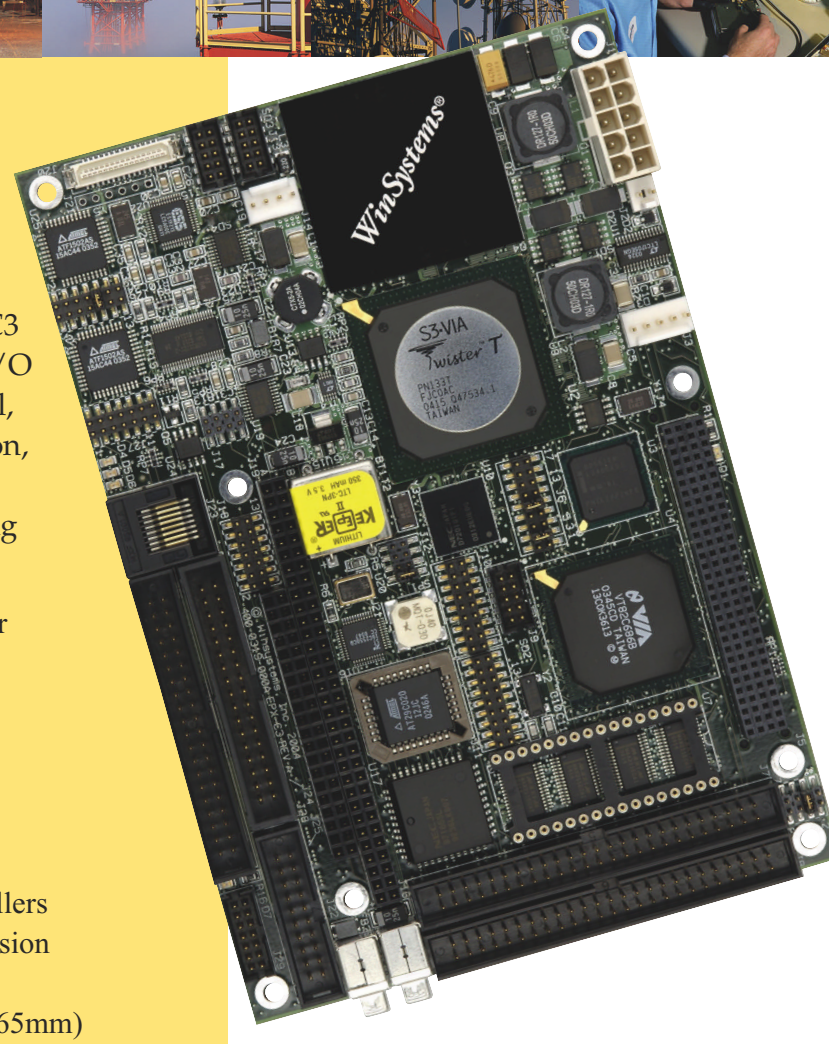


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## Microcontrollers build in support for off-chip SDRAM and flash

ARM7-core-based microcontrollers, smaller and consuming less power than ARM9-core devices, are workhorses for low-power embedded-system applications operating from batteries. However, to take advantage of built-in support for SDRAM, NAND flash, and CompactFlash off-chip memories, designers have had to use ARM9 or equivalent microcontrollers.

Addressing the desire to use ARM7, Atmel's new AT91SAM7SE512, SAM7SE256, and SAM7SE32 microcontrollers bring built-in support for these off-chip memories to ARM7 applications. The EBI (external-bus-interface) controller supports 32-bit off-chip memory in TrueIDE mode, and it includes an integrated ECC (error-correction-code) coprocessor for NAND flash. The larger memory supports features such as multilanguage data that you load at runtime or more extensive data logging for applications such as portable heart monitoring.

Using systems with external memory entails additional security risks, so the SAM7SE devices employ techniques to protect the system from malicious actions. For example, the microcontrollers boot only from internal memory. Also, the devices employ a flash security bit that disables the fast-flash-programming interface and JTAG access to the on-chip flash memory. In addition, the memory-protection unit in the devices can limit code execution from on-chip flash to prevent executing code directly from external memory. The on-chip flash uses a dual-bank architecture to support a true read-while-write capability and to offer additional protection to the system from power loss or cable disconnections when using the in-application programming for firmware upgrades.

The SAM7SE supports a migration path for SAM7S users by maintaining software compatibility. The new devices expand the general-purpose-I/O count from 32 to 88 pins to accommodate the EBI or to enable use of the devices' on-chip peripherals without multiplexing the peripherals when the EBI is not in use. The EBI supports a static-memory interface with built-in support for multiple chip select to facilitate interfacing to FPGAs. The SAM7SE devices also include an 11-channel peripheral-DMA controller with three programmed-I/O controllers to offload the data-movement processing from the CPU, including directly storing streaming data in the external memories.

On-chip communication interfaces include three USARTs, USB, TWI (two-wire interface), I²S, and SPI. The SAM7SE512 also includes four PWMs; an eight-channel, 10-bit ADC; three 16-bit timers; a watchdog timer; a real-time clock; a crystal oscillator; and supervisory features like those on 8-bit microcontrollers, including brownout detection and power-on-reset.

The AT91SAM7SE512, including 512 kbytes of on-chip flash, is available now in 128-pin "green" QFP or BGA packages and sells for $8.43 and $9.38, respectively (10,000). The AT91SAM7SE256 and AT91SAM7SE32 with 256 or 32 kbytes of on-chip flash will be available in early 2007.

**—by Robert Cravotta**

▷**Atmel**, www.atmel.com.

## 100-MHz to 1-GHz LXI scope modules provide two or four analog, 16 logic-timing channels

If you think that a scope with a huge display can't fit into 1¾ in. of rack space, think again. Scopes with external displays can accomplish this feat. The display can be part of a PC, but no PC is necessary if the scope provides its own 1024×768-pixel XGA interface to popular video monitors. Agilent takes this approach in its 6000L series of two- and four-channel, 100-MHz-, 500-MHz-, and 1-GHz-bandwidth LXI Class C DSO (digital-storage-oscilloscope) modules with optional 16-channel MSO (mixed-signal-oscilloscope) capabilities. Memory depth is 8M points/channel on two-channel units and on four-channel units in the two-channel (interleaved) mode. The scopes provide the manufacturer's MegaZoom feature for detailed viewing of fine details in long waveform records.

Prices, including software that provides full control over the units, range from $9695 for a two-channel, 100-MHz module that takes 2G samples/sec/channel and has no MSO capabilities to $23,195 for a four-channel, 1-GHz-bandwidth instrument that takes 4G samples/sec/channel in interleaved mode and includes MSO capabilities. You can add MSO capabilities to any 6000L scope without returning the scope to the factory or even using a screwdriver; you merely have to purchase and enter the software key that enables the feature. For applications in which data security is paramount, you can purchase the units with a factory-installed secure environment at no additional cost.

The 6000L units target use in test systems in which rack space is usually at a premium. Because nearly all such systems include a suitable display, the scope's screen generally adds no cost and takes no extra space. When you use the XGA port, the LXI scopes are fully compatible with the manufacturer's 6000A series and even offer some extra features. The rear panel houses Ethernet, IEEE 488, and USB 2.0 interfaces; the XGA output; trigger inputs; and the connector for the 16 digital MSO inputs. The front panel hosts the analog inputs; status indicators; an intensity control; and a second USB 2.0 connector, which makes it convenient to use a USB memory stick for waveform capture.

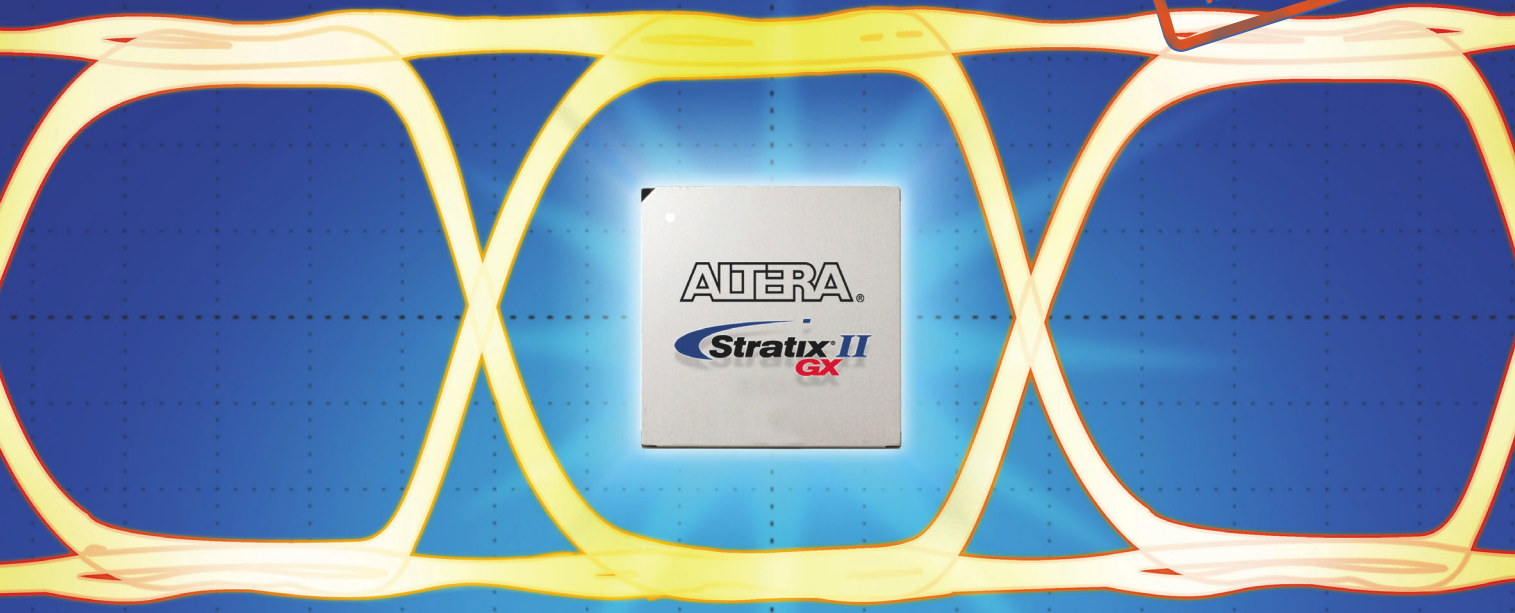
**—by Dan Strassberg**

▷**Agilent Technologies**, www.agilent.com/find/6000L.

By using a separate monitor, you can fit three four-channel LXI scopes in just 60% of the rack space that only one functionally equivalent benchtop unit occupies.

# The FPGA Eye Opener!

6.375-Gbps Transceivers Now Shipping!




Transmit eye diagram at 6.375 Gbps. For characterization details, see www.altera.com/stratix2gx/characterization.

## The complete transceiver solution with best-in-class signal integrity.

Stratix® II GX FPGAs offer the industry's most comprehensive solution for high-speed serial applications. With significantly lower power consumption than competing devices, Stratix II GX FPGAs have up to 20 transceivers performing with exceptional noise immunity from 622 Mbps to 6.375 Gbps. Designers have immediate access to Quartus® II software support and an array of intellectual property (IP) cores, system models, development boards, and collateral—everything needed to complete a design in the shortest amount of time.

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- **Low power consumption (140 mW/channel at 3.125 Gbps and 240 mW/channel at 6.375 Gbps) while retaining best-in-class jitter performance**
- **Dedicated circuitry supporting wide range of protocol standards across multiple data rates**

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# Multiflow USB controller optimizes handset data flow

Almost every mobile handset these days includes a target USB interface that users can employ to link a PC and the handset. For applications such as sporadically updating a handset's contacts, a relatively simple USB implementation serves well. But Cypress argues that, because more and more handsets feature multimedia capabilities and cameras, those features require the USB connection to achieve 480-Mbps data rates and to achieve that performance in a variety of multitasking scenarios. That theory led Cypress to develop the Antioch IC, which is both a USB and a mass-storage controller and the first member of Cypress' West Bridge family of USB-centric chips.

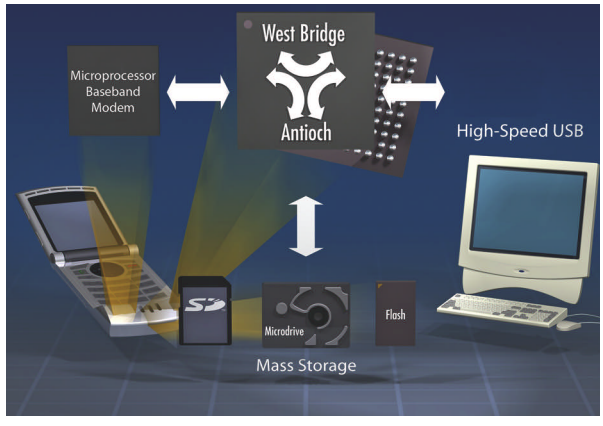
Cypress claims that the family targets embedded-USB applications, although this first offering clearly targets handsets. Non-USB designers may also find the chip useful because it takes a multiflow approach—somewhat akin to how multiport memory works—to USB operations. Cypress drew on its experience in both the USB and the multiport-memory areas in developing Antioch.

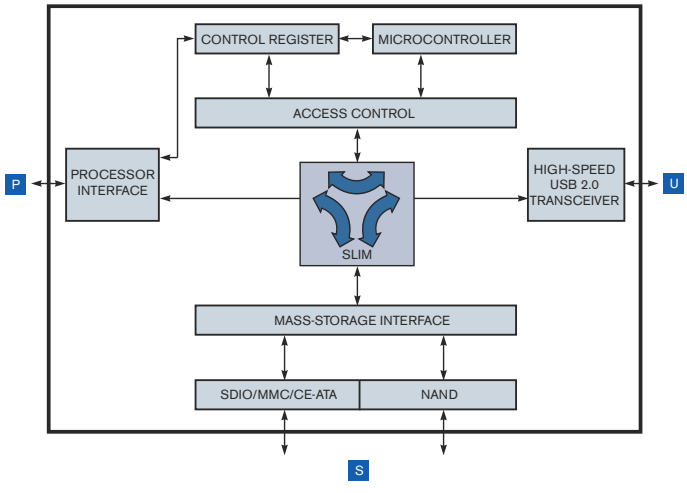
Why does a handset need Antioch when handset chips generally already support USB? Antioch sits between the handset application processor, the external USB interface, and some type of storage facility—most likely a hard disk or a flash memory. The architecture allows data to flow between any of the three connection points. Moreover, data flow doesn't rely on the handset processor. So, unlike in many other multimedia handsets, Antioch would allow users, for example, to download music from the PC into the handset's mass storage while talking on the phone. Cypress terms the multiflow architecture SLIM (simultaneous link to independent multimedia).

Cypress also claims that Antioch adds value in supporting all of the latest storage interfaces—such as SDIO (Secure Digital I/O), MMC+ (Multimedia Card Plus), and E-ATA (Embedded ATA)—whereas USB implementations in handset chips typically lag behind in their support of the latest technologies. The IC also includes a NAND-flash controller, a USB transceiver, and 16 configurable USB endpoints. Cypress plans to begin production shipments in the first quarter of next year at a price of less than $4 (500,000).

**—by Maury Wright**

▷**Cypress Semiconductor**, www.cypress.com.




A multiport data-flow engine lies at the heart of Cypress' Antioch USB and mass-storage controller that targets multimedia-capable handsets.

## ZIGBEE TRANSCEIVER OFFERS PROTOCOL FLEXIBILITY

12.01.06

**Microchip has just introduced the new IEEE-802.15.4-compliant MRF24J40 wireless transceiver, which supports both ZigBee and lighter weight protocols. Designers can use the transceiver with Microchip's MiWi (Microchip-wireless) stack, which the company offers free with its microcontrollers. In addition, the company announced the Zena graphical-network-analyzer tool, which designers can use to configure the ZigBee or MiWi protocol stacks. The transceiver is available for sampling now at $2.99 (10,000).**

**—by Maury Wright**

▶**Microchip Technology, www.microchip.com.**

## FROM THE VAULT

**"Predictions of things to come at this time of year stream across our desk in large numbers, and sometimes these prophecies make science fiction seem pretty tame."**

—Milton S Kiver, Editor, *EDN*, January 1957

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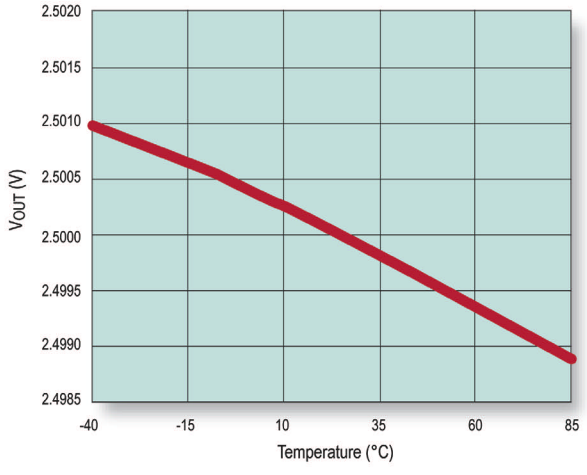
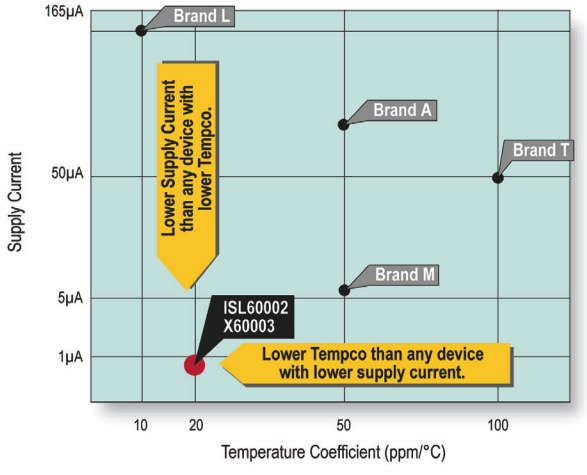
**$V_{OUT}$ ACCURACY vs TEMPERATURE NORMALIZED TO 25°C (Output = 2.5V)**




**TEMPERATURE COEFFICIENT vs SUPPLY CURRENT**




**ISL60002 and X60003 Key Parameters**

| Description | Conditions | Device Grade | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| Initial Accuracy | @25°C | B | -1.0 | | +1.0 | mV |
| | | C | -2.5 | | +2.5 | mV |
| | | D | -5.0 | | +5.0 | mV |
| Tempco | -40°C to +85°C | | | | 20 | ppm/°C |
| Supply Current | -40°C to +85°C | | | 350 | 700 | nA |
| Input Range | -40°C to +85°C | | 2.7 | | 5.5 | V |
| Long Term Drift | ΔTA = 25°C | | | 10 | | ppm/√1kHrs |

Datasheet, free samples, and more information about Intersil's entire family of Voltage References available at **www.intersil.com**

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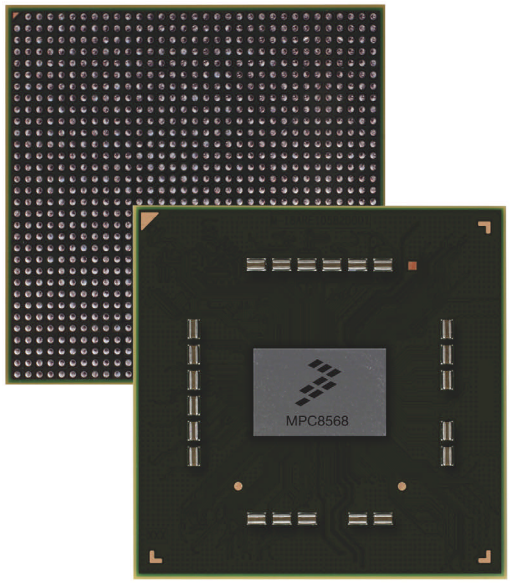


The PowerQuicc III encompasses the MPC8568E and MPC8567E, both including a Power Architecture core and supporting clock speeds as high as 1.33 GHz.

GLOBAL DESIGNER

# Communications processors support ZigBee 2006

The PowerQuicc series of communications processors from Freescale Semiconductor has evolved over many years. The latest generation of devices, PowerQuicc III, meets the needs of broadband-network-infrastructure equipment, such as 3G- or next-generation cellular or WiMax base stations. The company shaped the device's features to handle the multiprotocol-interworking tasks in applications such as gateways and ATM (asynchronous-transfer-mode), TDM (time-division-multiplexing), and IP (Internet Protocol) equipment, in which packet-based IP traffic coexists with legacy formats.

This release encompasses the MPC8568E and MPC8567E, both including a Power Architecture (PowerPC) core from the e500 series and supporting clock speeds as high as 1.33 GHz. The core has 512 kbytes of Level 2 cache and has a benchmark performance of as many as 3000 Dhrystone MIPS. It communicates with the outside world through on-chip Gigabit Ethernet, PCI Express, and Serial RapidIO interfaces. The E designation in the part numbers indicates that both chips have hardware-security features that support the execution of a range of encryption algorithms on the fly.

New in the III series is the Quicc engine, a programmable-function block that provides hardware acceleration of the primitive operations specific to communications protocols, such as ATM, POS (Packet over SONET), Ethernet, PPP (Point-to-Point Protocol), HDLC (High-Level Data-Link Control), and TDM, offloading the general-purpose Power Architecture core. The chip also includes a table-look-up unit, a DDR memory controller, and a hardware floating-point unit. Freescale provides standard microcode for established protocols and downloadable updates for new and evolving ones. Development is on the CodeWarrior software platform. The chips will cost $100.80 (10,000).

Addressing the slower end of the data-communications-speed range, Freescale's Jon Adams, director of radio technology and strategy in the company's wireless- and mobile-systems group, comments on the recent revision to the ZigBee specification: "The changes the ZigBee Alliance [www.zigbee.org] has made are essential to allow ZigBee deployment as the alliance intended. The revision process focused on the top four issues that developers had identified." For example, although the ZigBee outline specification in principle allows for 216 nodes, a network could in practice handle only those networks with 100 or fewer nodes. The changes, which include modifications to the procedures for address allocation, extend that capability to allow ZigBee to handle thousands of nodes, which, Adams says, real-world industrial networks will require.

> ZigBee product development will soon enjoy a new impetus, with activities beyond the technology market.

Other changes improve areas such as security; Adams believes that ZigBee product development will soon enjoy a new impetus, with activities beyond the technology market. These activities could include progress on branding for products at the consumer level. The ZigBee Alliance has discussed the merits of a single ZigBee brand as opposed to brand identification specific to different product sectors. Freescale has a variety of ZigBee products: both separate radio and baseband architectures and "single-package" offerings. The company declines to disclose whether the single package is a single RF and baseband die or a multichip package. The company also sells 802.15.4 products without the ZigBee protocol stack if you want to develop a proprietary device or an even more basic 802.15.4 radio offering. Freescale is about to announce a ZigBee software stack that it has developed entirely in-house. (The company previously used a third-party product.) The new stack will fully comply with the 2006 revision. A bill-of-materials cost for this ZigBee module will be $4 to $4.50 (10,000).

**—by Graham Prophet, *EDN Europe***

▷**Freescale Semiconductor**, www.freescale.com.

# Intersil Analog Switches

High Performance Analog

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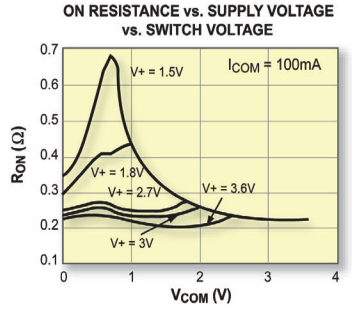
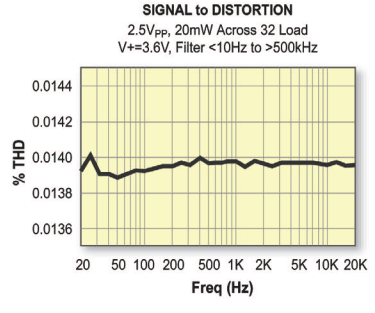
| | Device | Function | $R_{ON}$ @ 2.7V (Ω) | $R_{ON}$ Flatness (Ω) | ESD (HBM) | Supply Voltages (V) | Packages |
|---|---|---|---|---|---|---|---|
| Singles | ISL84714 | SPDT/2:1 Mux | 0.44 | 0.06 | 6kV | 1.6 to 3.6 | SC70-6 |
| | ISL84715 | SPST (NO) | 0.26 | 0.04 | 4kV | 1.6 to 3.6 | SC70-5 |
| | ISL84716 | SPST (NC) | 0.26 | 0.04 | 4kV | 1.6 to 3.6 | SC70-5 |
| | ISL43L210 | SPDT/2:1 Mux | 0.44 | 0.06 | 6kV | 1.1 to 4.5 | SC70-6 |
| | ISL43L110 | SPST (NO) | 0.26 | 0.04 | 4kV | 1.1 to 4.5 | SC70-5 |
| | ISL43L111 | SPST (NC) | 0.26 | 0.04 | 4kV | 1.1 to 4.5 | SC70-5 |
| Duals | ISL84762 | 2xSPDT/2:1 Mux | 0.29 | 0.03 | 9kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL84684 | 2xSPDT/2:1 Mux | 0.29 | 0.03 | 9kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL8484 | 2xSPDT/2:1 Mux | 0.29 | 0.03 | 9kV | 1.6 to 4.5 | TDFN, MSOP |
| | ISL43L220 | 2xSPDT/2:1 Mux | 0.23 | 0.03 | 9kV | 1.1 to 4.5 | TDFN |
| | ISL43L410 | DPDT/Diff 2:1 Mux | 0.29 | 0.03 | 9kV | 1.1 to 4.5 | TDFN, MSOP |
| | ISL43L120 | SPST (NO) | 0.17 | 0.008 | 8kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL43L121 | SPST (NC) | 0.17 | 0.008 | 8kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL43L122 | SPST (Mix) | 0.17 | 0.008 | 8kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL43L710 | Diff SPST (NO) | 0.17 | 0.008 | 8kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL43L711 | Diff SPST (NC) | 0.17 | 0.008 | 8kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL43L712 | Diff SPST (Mix) | 0.17 | 0.008 | 8kV | 1.6 to 3.6 | TDFN, MSOP |
| Quads | ISL83699 | Dual DPDT/Diff 2:1 Mux | 0.3 | 0.06 | 9/4kV | 1.6 to 3.6 | QFN, TSSOP |
| | ISL84780 | Dual DPDT/Diff 2:1 Mux | 0.45 | 0.07 | 4kV | 1.6 to 3.6 | TQFN, TSSOP |
| | ISL8499 | Dual DPDT/Diff 2:1 Mux | 0.3 | 0.06 | 9/4kV | 1.6 to 4.5 | QFN, TSSOP |
| | ISL43L420 | Dual DPDT/Diff 2:1 Mux | 0.3 | 0.06 | 9/4kV | 1.1 to 4.5 | QFN |
| Octals | ISL84781 | 8:1 Mux | 0.41 | 0.056 | 4kV | 1.6 to 3.6 | TQFN, TSSOP |
| | ISL84782 | Diff 4:1 Mux | 0.5 | 0.056 | 4kV | 1.6 to 3.6 | TQFN, TSSOP |
| | ISL43L840 | Dual 4:1 Mux | 0.5 | 0.056 | 4kV | 1.6 to 3.6 | QFN, TSSOP |
| | ISL43L841 | Diff: 4:1 Mux | 0.5 | 0.056 | 4kV | 1.6 to 4.5 | TQFN, TSSOP |

## ISL84684 Typical Performance

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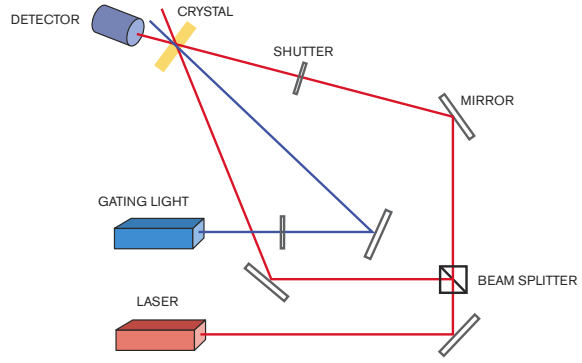



In this experimental setup, a spatial-light modulator would work in the shutter location. In practice, the crystal would be the surface layer of a holographic disk.

RESEARCH UPDATE

BY RON WILSON

# Ferroelectric LCD enables holographic recording

Holographic-data storage has been one of the continuing research quests that always seems to have great theoretical merit but even greater implementation problems. In principle, the technology allows you to store a pattern on an optical-recording medium in a highly compressed format by printing an optically reduced holographic image of the pattern onto the material. If the pattern is a 2-D array of pixels, such a technique can store random binary data. But finding an appropriate recording medium, appropriate laser, optically stable yet inexpensive light paths, and a suitable device for generating the patterns in the first place have all been problematic.

Now, ferroelectric-liquid-crystal specialist Displaytech has announced a new liquid-crystal-light valve for use in generating the optical patterns for holographic-data recording. The SLM (spatial-light modulator), a 1216×1216-pixel array of liquid-crystal cells, modulates polarized light from a blue laser to create the data beam for optical recording in a holographic medium.

Displaytech claims that the device suits holographic-recording applications because it employs ferroelectric technology within the liquid-crystal cells, which makes possible the device's high switching rate and allows it to sustain a 1.1-kHz frame rate.

You feed data to the SLM in roughly 1-Mbit blocks, setting the binary states of the pixels. Flashing a laser along two paths, a reference path directly onto the surface of an optical disk and a datapath through the SLM, causes the recording of an interference pattern, much smaller than the area of the SLM, onto the disk. This pattern contains all of the information necessary to construct the original 1216×1216-pixel pattern of ones and zeros.

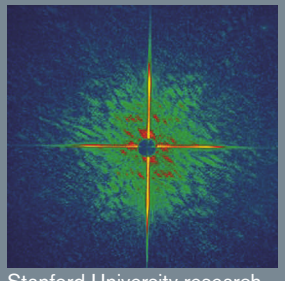
The high frame rate of the SLM allows you to more quickly record frames on the disk. And the fact that the SLM area is small makes the modulator a good fit for the geometry of optical-holographic-disk prototypes. (Previous applications for Displaytech's ferroelectric LCDs include displays on digital cameras and in goggles.) The device needs no extreme optics to reduce the area of the light beam passing through a large modulator to the small area on the disk.

▷**Displaytech**, www.displaytech.com.

## X-RAY-IMAGING CONCEPT MAY REVEAL SINGLE NANOSCALE STRUCTURES

**A free-electron laser, which has emerged as a new kind of X-ray-photon source, may address the limitations of conventional X-ray-diffraction techniques, according to recent results from Stanford University. They get their power from high-energy electron sources. The devices can output staggering amounts of power: Stanford researchers estimate that a free-electron laser that the university is now constructing at SLAC (Stanford Linear Accelerator) will be 10 billion times more intense than any existing X-ray source on earth.**

**Such intensities make it theoretically possible to obtain an X-ray-diffraction pattern from a single nanoscale object. The device would diffract enough energy from the object for sensors to record. Unfortunately, such intensity also means that the object in question would lose its electrons and reach almost immediate destruction, so only a tiny window would be available in which to capture the diffraction pattern before the object in question became a dispersing cloud of plasma. You may suspect that, given this limitation, weapons-related applications for free-electron lasers emerge, as well, if researchers can address the inconvenience of the energy source.**



Stanford University researchers created this X-ray-diffraction pattern from a nanoscale object.

**An international team of researchers, led by Stanford professor Janos Hajdu, has solved this problem. Mathematical models predicted that a sufficiently fast burst of X-ray photons would allow sensors to capture a diffraction image before the object dispersed.**

**Using a free-electron laser at Deutsches Elektronen-Synchrotron in Hamburg, Germany, the researchers verified by careful tuning that an intense 25-fsec pulse from the laser was sufficient to create an image.**

**▶Stanford Linear Accelerator, www-ssrl.slac.stanford.edu.**

**▶Deutsches Elektronen-Synchrotron, www.desy.de.**

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|---|---|---|---|---|---|---|
| FPGA | √ | | | | | |
| Toshiba IP Platform SoC | √ | √ | √ | √ | √ | √ |
| Pure-Play Foundry | | | √ | | √ | √ |
| Toshiba Foundry | | √ | √ | √ | √ | √ |

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TOSHIBA

BY HOWARD JOHNSON, PhD

# Eye of the probe

My differential probe touches two surface-level signal traces, directly adjacent to the input balls of a 2.5-Gbps digital deserializer in a large BGA package (**Reference 1**). The signal arrives from an optical-to-electrical converter some 6 in. away.

**Figure 1** illustrates one-half of that measurement setup as a single-ended circuit, omitting all complementary differential-circuit elements.

Capacitor $C_3$ represents the surface-mount soldering pad and ball at the periphery of the BGA package. Inside, the signal traverses 1.25 in. of internal BGA-substrate routing before reaching an on-die end termination and the input capacitance, $C_4$, of the receiver.

In this circuit, I suspect, my probes significantly affect the measurement. To test that theory, I took the measurement first using one and then two probes in tandem.

The two probe models in **Figure 1** each depict one complementary half of a differential probe. For Probe 1, the model includes three parts. Inductor $L_1$ represents the size and shape of the probe tips. Internal resistor $R_1$ damps internal resonances.

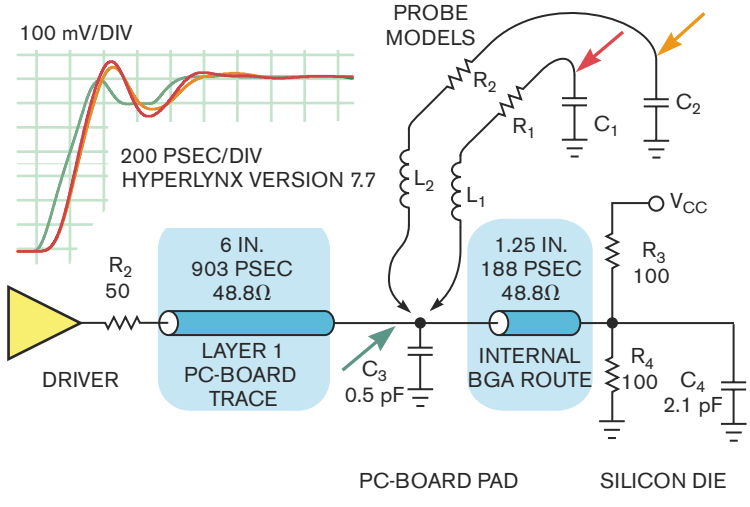


Figure 1 A second probe changes the observed waveform.

High-end probes often include such a resistive feature. Capacitor $C_1$ models the overall input capacitance of the probe head. The voltage at $C_1$ is the voltage that Probe 1 "sees." The voltage at $C_2$ is the voltage that Probe 2 sees. Your probe manufacturer may have a different circuit that best represents the effects of your probe. With only Probe 1 connected, **Figure 1** plots the voltage at $C_1$ in red. Now, connect Probe 2. Adding Probe 2 to the circuit changes the voltage at $C_2$ and $C_1$ to the orange waveform. Obviously, the second probe affects the results, confirming my suspicions. Each probe loads the circuit and corrupts the physical measurement.

So, how can you discern the "real signal" at $C_3$ with no probes attached? The purpose of simulation is to make this determination. By crosschecking physical and simulation techniques, you can overcome many measurement deficiencies.

First, work on the accuracy of your modeling until your simulated waveforms with a simulated probe match physical measurements taken through the eyes of a physical probe. Once you achieve that correlation, you may infer that the simulated waveform with no probes attached (green waveform) is the real McCoy. EDN

## REFERENCE

1 Johnson, Howard, "Eye don't like it," *EDN*, Nov 9, 2006, pg 34, www.edn.com/article/CA6387033.

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**Go to www.edn.com/061201hj and click on Feedback Loop to post a comment on this column.**

*Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.*

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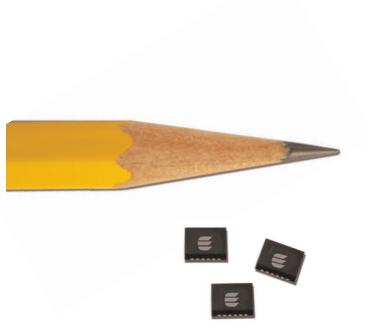

- ☑ Deterministic TDMA protocol
- ☑ Bit rate: 312.5kbps
- ☑ Scan time for 32 devices: ≤25ms
- ☑ Wire type: 16AWG (1.3mm) to 24AWG cat5 (0.5mm)
- ☑ 24VAC or DC power and data on two wires
- ☑ Application power delivered to each device: 100mA@3.3VDC
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BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

# Your mileage may vary

I've been enjoying relief from our high gasoline prices thanks to the HEV (hybrid-electric vehicle) I've been driving. Among the car's features is a display that provides the instantaneous mileage, the integral of that measure over each of the six most-recent five-minute intervals, and the integral since the last reset, which I initiate after refueling.

With so much information at hand, drivers can learn how their driving style influences fuel economy. I've used the display as a biofeedback system to learn how to squeeze the most mileage out of the fuel I've used, and, in all modesty, I think I've become pretty good at it. On a tank of gasoline, I can easily average in excess of 45 mpg—more than 50 mpg with care. Overall, I'm elated … with one sticking point.

My vehicle's EPA (Environmental Protection Agency)-estimated mileage is 51 mpg on the highway (**Reference 1**). The HEV's city-mileage rating is 60 mpg, however, and that number, though attainable for short runs, is simply hokum as a representation of sustainable performance.

The problem isn't with me, my vehicle, HEVs, or vehicles made by a given manufacturer; the problem is the dissimilarity between the conditions under which the manufacturers and the EPA's National Vehicle and Fuel Emissions Laboratory collect data and those under which you and I drive. Prompted by research from Consumers Union, the publishers of *Consumer Reports*, the EPA announced last January that it will revamp its fuel-economy-ratings data-collection method for the first time in 20 years, effective with 2008 models (**references 2** and **3**). Expect falling estimates.

Perhaps the best deadpan line on the subject appeared in *The New York Times*, which quoted Toyota spokesperson Martha Voss: "The ratings might change, but the performance of our customers' cars won't change" (**Reference 4**). For anyone who has spent considerable time pouring over specifications and designing to parametric goals, this statement seems almost perfect in how upside down it is.

Yet it reminds me of an ongoing challenge that OEM designers face when working with a vendor's data sheets, particularly those for analog and mixed-signal ICs, the behaviors of which tend to be highly parametric. Given the cost of production testing—a large fraction of an IC's *full-factory cost*—vendors must test a reasonable number of parameters over an affordable set of conditions. From the OEM designer's perspective, IC specifications *and* the conditions under which they apply must be *relevant*, *realistic*, and *reproducible*.

**Relevant:** Test conditions must include the range under which the IC will operate in your product. It sounds obvious, but IC makers cannot predict the specific environment your product presents to theirs. So you must confirm that their test conditions are relevant to the environment your product will provide or, as they say, "your mileage may vary"—and not in ways that are dependable or easy to predict.

**Realistic:** IC makers are usually clear on how OEMs are likely to use their products and accordingly develop test suites. Read carefully, however, for specifications written with test conditions that vary for particular parameters. Determine whether these are realistic within the context of your design. Your product's performance simultaneously depends on all critical specs.

**Reproducible:** Though you shouldn't need to second-guess an IC maker's data sheet, you should be able to confirm critical specifications on the bench. As ICs provide greater functional density and increasing bandwidths, you must be able to confirm that your layout does not present strays or coupling paths that compromise the performance that your IC selection promises. Vendors' layout recommendations and evaluation boards can reduce your design's risk of failure and provide a solid reference for comparison for little cost or effort. EDN

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*Contributing Editor Joshua Israelsohn is director, technical information for International Rectifier. Contact him at edn-joshua@sbcglobal.net.*

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No. 115



# Implementing Single-Chip FPGA Power Solutions

*— By Hector F. Arroyo, Sr. Field Applications Engineer*

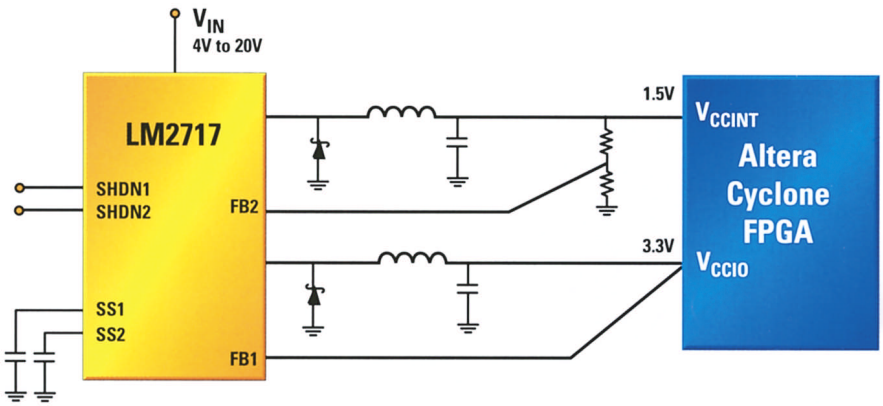


**Figure 1.**
**LM2717 Dual Integrated Switching Supply for 1.5V Core and 3.3V I/O Medium-power FPGA**

FPGA-based systems are becoming increasingly common. While many designers favor FPGA-based architectures for the flexibility of adding features or making modifications through code, designing an adequate power supply involves some challenges. First is the multiple power rail issue. FPGAs require, as a minimum, one voltage for powering the core and one (or more) voltages to power the I/O banks. However, FPGA-based systems may require additional rails to power double data rate (DDR) memory, transceivers, Ethernet Physical Layer ICs (PHYs), ADCs or small microcontrollers. Additionally, these voltage rails need to have specific characteristics: sub-1.25V outputs, monotonic ramp-up, sequencing, and controlled rise time etc.

While design engineers and semiconductor manufacturers make continuous efforts to provide integrated, easy-to-use alternatives, many times it is still up to the designer to leverage available features and go beyond the typical datasheet circuit to implement an optimal solution. Through this article, we

**NEXT ISSUE:**
**Powering High Brightness LEDs**

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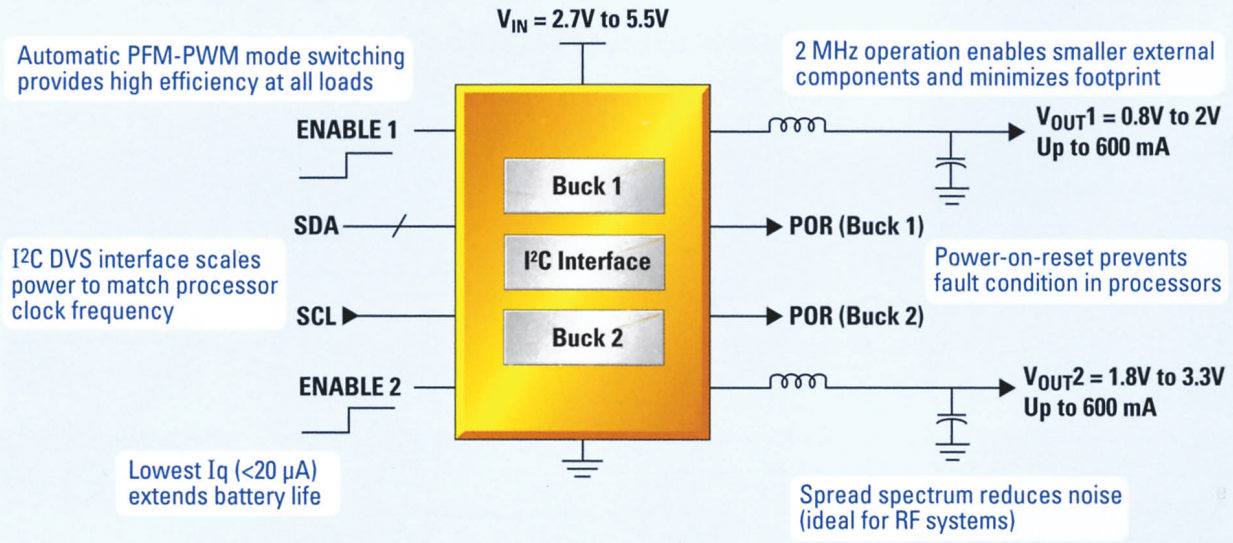
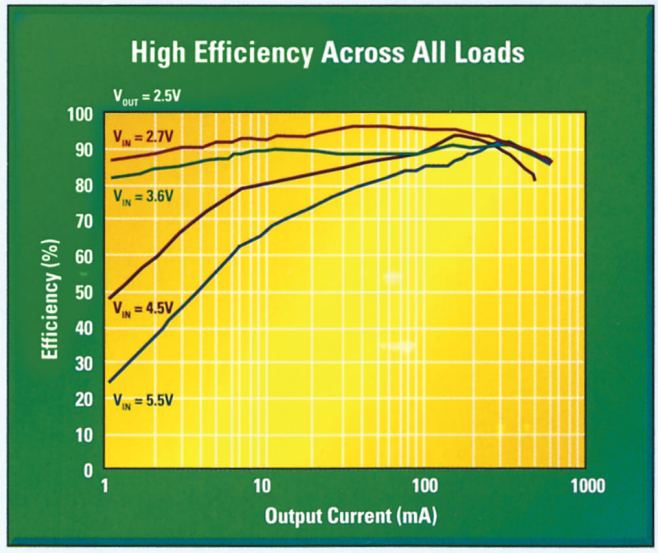
*The Sight & Sound of Information*

# Enhance Digital Processor Power Management with Dynamic Voltage Scaling (DVS)

## LM3370 Dual Buck Regulator Provides Highest Efficiency for FPGAs and Multimedia Processors




Ideal for low-power FPGAs, CPLDs, and application processors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**www.national.com/pf/LM/LM3370.html**

# Implementing Single-Chip FPGA Power Solutions

will explore some available multi-output regulators that can be used as single-chip FPGA power supplies and techniques on how to implement sub-1.25V outputs from readily available bandgap regulators.

*Figure 1* shows a simplified diagram of a typical application to power an FPGA (like a Cyclone device from Altera) with a single-chip power supply. National's LM2717, an integrated dual-output switching regulator IC, is set to provide 1.5V at 2A (3.2A peak) to the core and 3.3V at 1.5A (2.2A peak) to the I/Os.

The LM2717 is medium-power, single-chip solution with the simplicity and flexibility needed to implement a compact, greater than 90 percent efficient, supply matching the specifications for many digital multi-rail systems, including FPGAs, from a variety of sources: 5V, 12V or wall warts in the 4V to 20V range. The LM2717 comes with one adjustable output and one fixed output at 3.3V, a very common rail, which helps save space and increase output voltage accuracy by implementing internal output-voltage-setting resistors on this output. The LM2717-ADJ is a variation of the original LM2717 IC that allows both outputs to be adjustable, which is very useful if a different I/O voltage is needed.

Altera's literature on Cyclone and Cyclone II, as well as many other latest generation FPGAs such as Xilinx Spartan 3E, state that those FPGAs do not require any specific sequencing on their voltage rails during power-up. However, individual enable pins (SHDN1 & SHDN2) are still present on the LM2717 to turn on each output at a specific time or in a specific order should this be necessary for the system or when powering other FPGAs. In the same fashion, individual soft-start pins (SS1 and SS2) allow the LM2717 to set different ramp-up times for each output voltage to meet manufacturer specifications for individual FPGAs and other digital cores.

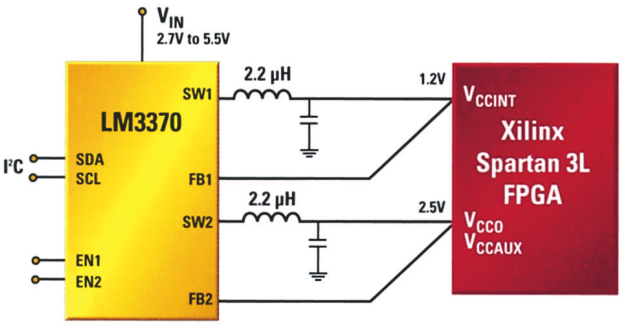


**Figure 2.**
**LM3370 Dual Integrated Synchronous Switching Supply for 1.2V Core and 2.5V I/O and $V_{CCAUX}$ Low-power FPGA**

*Figure 2* shows a low-power 1.2V, 90 nm FPGA (Spartan 3L from Xilinx) powered by the LM3370, a dual 600 mA per channel integrated synchronous buck regulator.

Voltage for one channel can be adjusted from 1V to 2V in 50 mV steps (ideal for core power) while the other channel can be programmed for an output of 1.8V to 3.3V in 100 mV steps (ideal for I/O power). Individual enable pins, internal soft-start, fast transient response, and power-on-reset flags for each output make this IC a single-chip minimum-external-components solution optimized to power low-power FPGAs and other multi-rail digital cores.

While the LM3370 can be used off-the-shelf because pre-programmed output voltages and individual enable pins are available. An on-board I²C-compatible interface allows the user to optionally modify various parameters of the IC, even dynamically, for added flexibility. These parameters include output voltage setting (per channel), output enable (per channel), switching mode selection (auto PWM-PFM for high efficiency under light-loads or fixed PWM for fixed frequency operation), spread spectrum feature enable, and spread spectrum frequency range selection.

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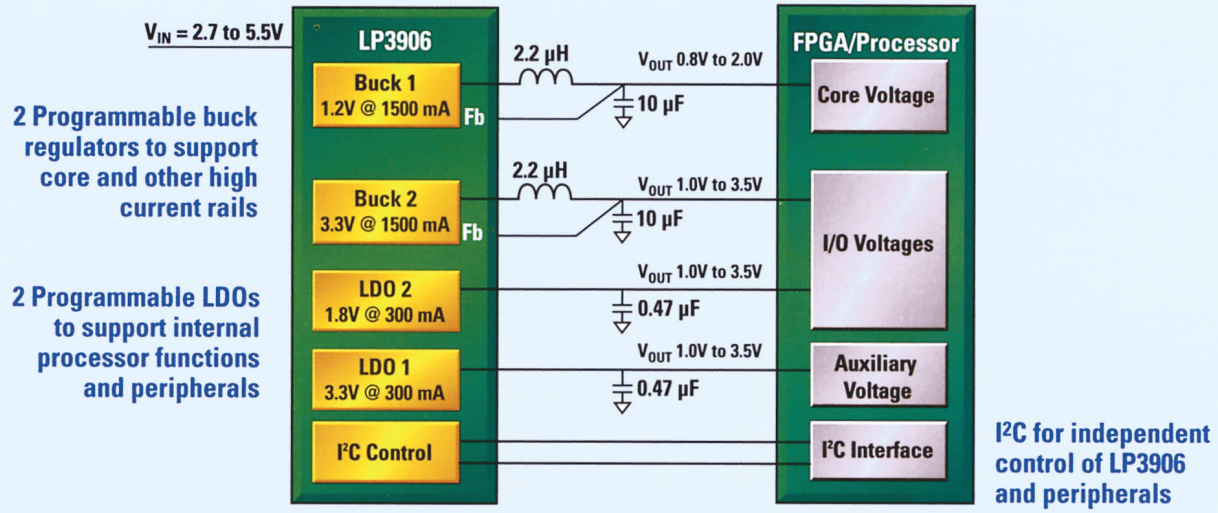


AVAILABLE LEAD-FREE

| Product ID | Digitally Programmable | Efficiency | Regulator Output Current | LDO Output Current | Packaging | Solution Size |
|---|---|---|---|---|---|---|
| LP3906 | I²C | Up to 96% | 1.5 A | 300 mA | LLP-24 | 20 mm x 20 mm |
| LP3905 | N/A | Up to 90% | 600 mA | 150 mA (low noise) | LLP-14 | 15 mm x 10 mm |

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# Implementing Single-Chip FPGA Power Solutions

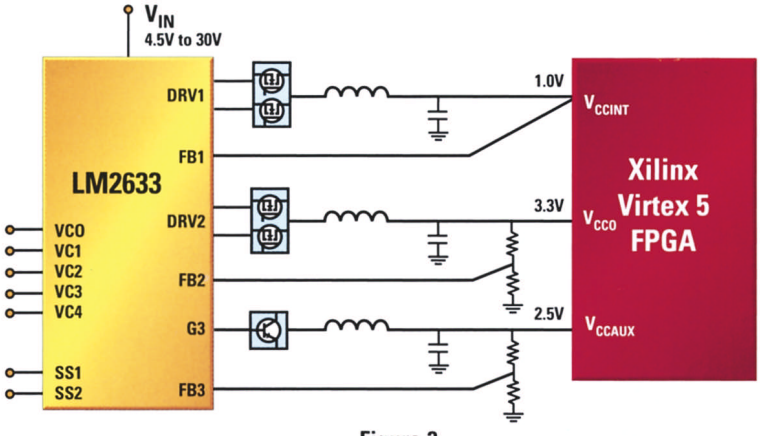



**Figure 3.**
**LM2633 Triple Switching/Linear Controller Supply for 1.0V Core, 3.3V I/O and 2.5V $V_{CCAUX}$ High-power FPGAs**

The simplified diagram in *Figure 3* shows the implementation of a three-rail, higher power FPGA supply. In this case, an LM2633 controller is providing 1.0V to a Xilinx Virtex 5 core, 3.3V to the I/Os and 2.5V for $V_{CCAUX}$. The LM2633 is a triple output IC, and is a perfect example of how existing technology can be leveraged for new purposes, taking it out of its original context. Two of the three LM2633 outputs utilize a synchronous rectification buck architecture to provide maximum efficiency to medium and high current loads (5A to 15A per channel) while it also integrates an LDO controller for a third low-power output. One of the switching outputs has a voltage range between 0.900 and 2.000, making it a perfect fit for powering the core of digital devices. The second switching output has a range of 1.25V to 6V, adequate for I/Os, memory, and other loads. For higher accuracy and flexibility, the low voltage output is programmable through a 5-bit parallel digital word that can be either hard-wired or tied to a processor for dynamic voltage scaling if desired.

For applications where only a dual synchronous buck controller with sub-1.25V outputs is needed, the LM2657 provides a good alternative in a fewer pin-count package. For lower power applications where three or four rails are needed, the LP3906 is also an excellent alternative, providing two fully integrated 1.5A synchronous switching outputs and two 300 mA LDO outputs, all in a single package.

As seen from the previous examples, most of today's FPGAs require 1.50V, 1.20V and sometimes even a lower core voltage (as Xilinx's newest Virtex 5 series of FPGAs which have a 1.0V 65 nm core). Many regulators in the market have a regular 1.25V bandgap reference. *Figures 4* and *5* show simplified diagram examples of how to use regular bandgap ICs (like the LM2717) to power such sub-bandgap digital loads. Fundamental operation of the voltage converter remains the same, but the way in which the resistive voltage divider is referenced to program the regulator's output voltage is different.

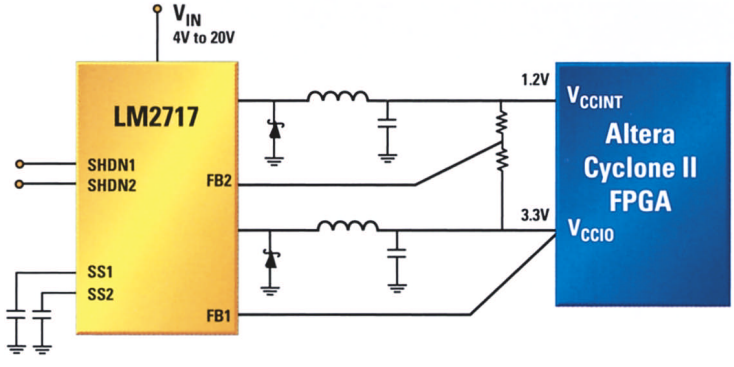
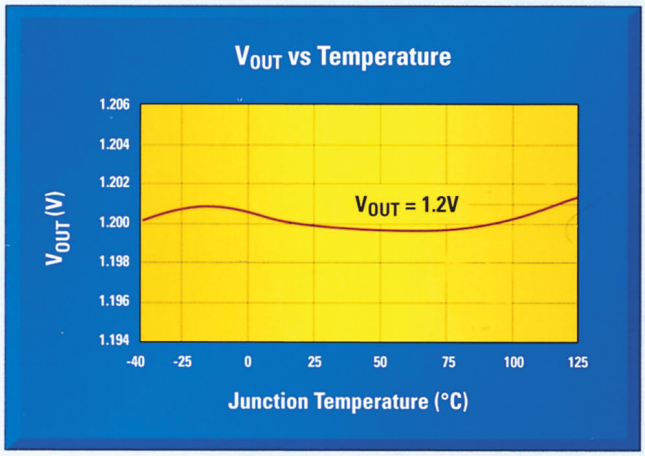
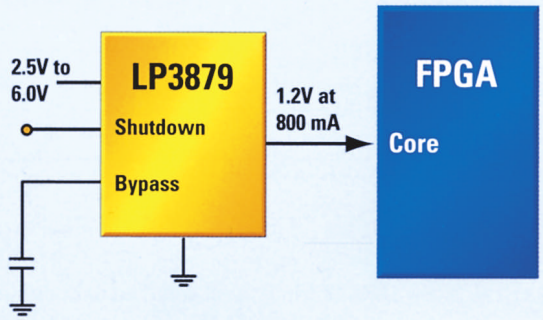



**Figure 4.**
**LM2717 1.2V Core, 3.3V I/O Dual Integrated Switching FPGA Supply Using the 3.3V Rail as Auxiliary Voltage for Sub-1.25V Core Voltage Generation**

# 1.2V Output LDO Enables Powering of Latest Generation Digital Cores

## LP3879 800 mA LDO Provides ± 1% Initial Output Accuracy




### LP3879 Features

- 1% initial output accuracy
- Input voltage: 2.5V to 6.0V
- Custom voltages available from 1.0V to 1.2V
- <10 µA quiescent current in shutdown
- Low 18 µV output noise reduces noise
- Available in PSOP-8 and LLP-8 surface mount packages

**LDOs for Powering FPGAs**

| Product ID | $V_{OUT}$ Range | $V_{IN}$ Range | $I_{OUT}$ | Features |
|---|---|---|---|---|
| LP38856 | 0.8V to 1.2V | 1.3V to 5.5V* | 3A | Enable Pin |
| LP38859 | 0.8V to 1.2V | 1.3V to 5.5V* | 3A | Soft Start Pin |
| LP3879 | 1V to 2V | 2.5V to 6V | 800 mA | Shutdown Pin |
| LP3878 | 1V to 5.5V | 2.5V to 16V | 800 mA | Adjustable Output |
| LP5951 | 1.3v to 3.3V | 1.8V to 5.5V | 150 mA | Low 29 µA quiescent current |

* 3V to 5.5V input bias rail required

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# Implementing Single-Chip FPGA Power Solutions

In any closed-loop regulator circuit, the output voltage, after being scaled down by a resistor divider, is compared to an internal reference. If this reference is 1.25V, then the scaled-down sample of the output voltage, which is injected to the regulator IC through the FB pin, needs to be set to match this value to maintain regulation. In a typical system, this FB voltage divider is placed between the output (highest potential) and ground (lowest potential) since the FB voltage (1.25V) falls within this range. In a system that requires the output voltage to be below the internal reference value, we still need to provide a matching voltage (1.25V) to the FB pin, however this value won't fall now between $V_{OUT}$ (which is now lower) and ground. The way to achieve it is by placing the voltage divider between $V_{OUT}$ (now becoming the lowest potential and the lower end of the divider) and any auxiliary voltage above 1.25V (to serve as the higher potential).

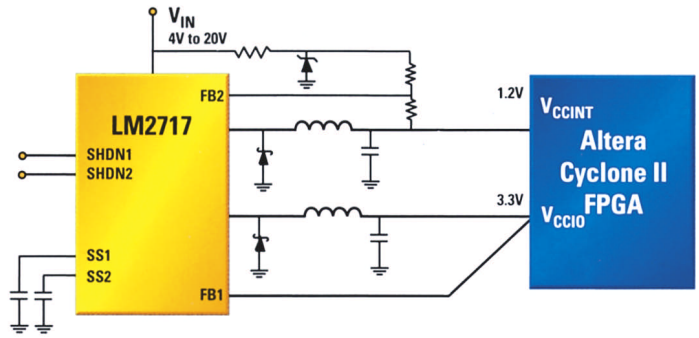



**Figure 5.**
**LM2717 1.2V Core, 3.3V I/O Dual Integrated Switching FPGA Supply Using an LM4040 Shunt Reference for Sub-1.25V Core Voltage Generation**

The example in *Figure 4* uses Altera's Cyclone II 1.20V FPGA and National's LM2717 to show the simplest implementation for this configuration, with the higher voltage being the 3.3V rail itself. Adequate filtering and layout for this rail is important (a decoupling ceramic capacitor close to where the resistive divider lower end meets the 3.3V rail is recommended) because regulation on the sub-bandgap output will depend on the stability of this rail. Sequencing is also important, because 3.3V rail needs to be present for proper regulation before the core voltage output is turned on.

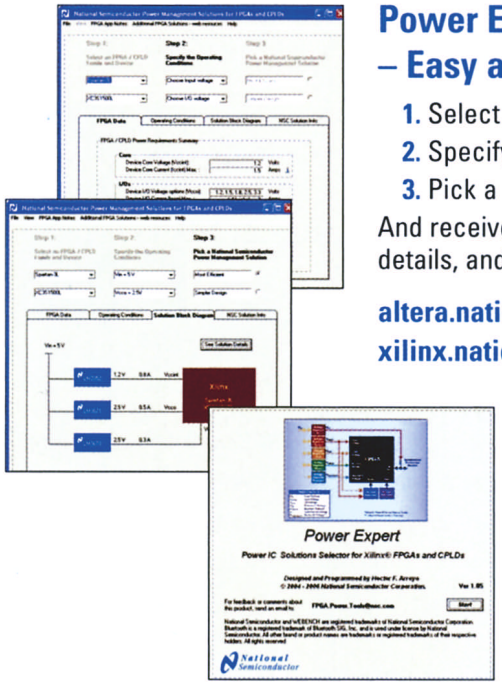
In most FPGAs, the nominal 1.20V or 1.0V core supply voltage needs to be stable within ±50 mV or ±60 mV, so all transients, ripple and tolerance variations need to be kept within that limit.

*Figure 5* shows an alternate method for achieving a sub-bandgap output using an independent source for the auxiliary rail, in this case a small, low-cost shunt reference (precision Zener), such as National's LM4040CIM3-2.5 (0.5%) or LM4040DIM3-2.5 (1%). This approach allows potential transients seen in the 3.3V output not to be cross-coupled to the regulation of the 1.20V output. It also allows the 3.3V rail to be powered up after the 1.2V rail, or be turned off at any time without disturbing the 1.2V output regulation. Accuracy of this output is dependent on the line regulation of the selected voltage reference. Because core voltage accuracy is important in the application, selection of the right voltage reference is key.

Multiple resources are available today to assist designers craft the optimal power supply for their application. For example, National's Power Expert software tool, easily guides the user through selecting the FPGA of their choice, picking up the supply rails and operating conditions and finally recommending the power IC solution that matches the designers top requirements, whether these are maximum efficiency or design simplicity. It also connects to National's WEBENCH® design environment for component selection around the selected regulator IC and circuit simulation (if these features are available for the selected regulator). ■

For additional information on these tools, visit **altera.national.com** and **xilinx.national.com**.

# Power Design Tools

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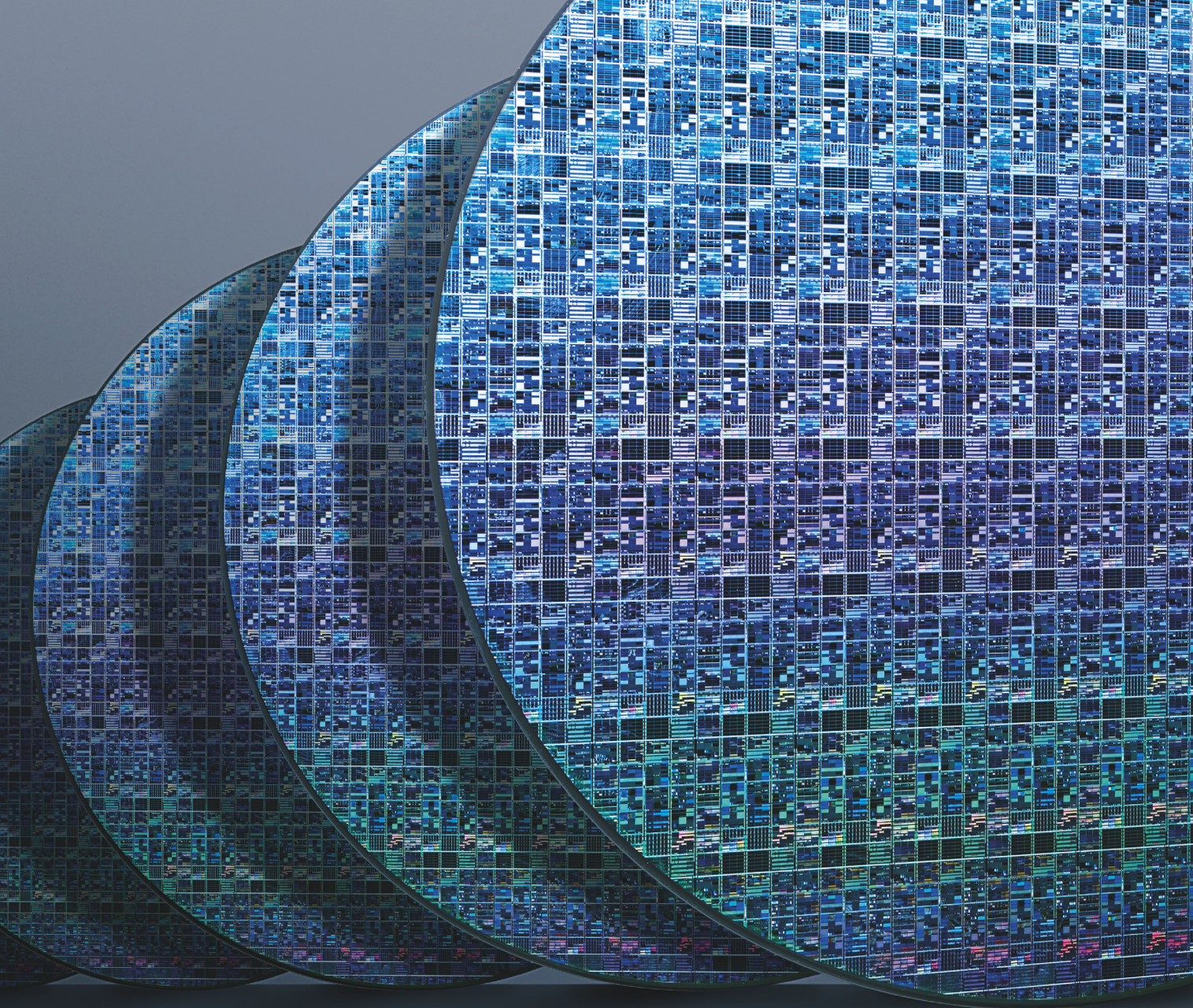

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# Flash memory shines brightly as code and data store

TECHNOLOGY MOVED FROM LOW-DENSITY SPECIALIZED APPLICATIONS TO THE MAINSTREAM.

Toshiba invented the flash-memory concept in 1984. But when *EDN* first covered real products four years later, the "flash" moniker had yet to take hold. Although it used the word "flash" in its headline, an Oct 27, 1988, *EDN* article, "Conventional EEPROMs and flash EEPROMs offer a spectrum of bit densities" (see the excerpt below and www.edn.com/article/CA6371935 for the full article), actually suggested that these new devices should be called "full-featured EEPROMs."

The article discussed mainly specialized applications for the relatively expensive form of rewritable memory. Fast-forward to 2006, and flash has enabled devices such as digital cameras and MP3 players that consumers would hate to do without.

As happened with other memory types, Intel became the first, in 1988, to commercialize the NOR flash that Toshiba had described in 1984. NOR flash features random-access capabilities and has found most success as a rewritable-code store. An updatable PC BIOS numbered among the first broadly successful applications.

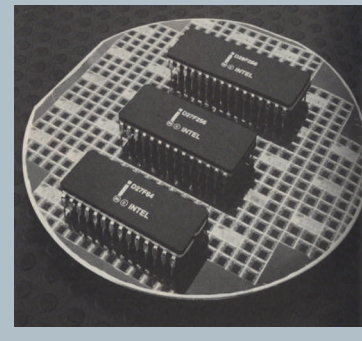
Toshiba followed up the NOR invention with the invention of NAND flash in 1989. Generally, NAND is cheaper, denser, and faster than NOR flash. But NAND flash does not support random access. Still, NAND flash, with its sequential read/write limitation, has proven perfect for data-storage in digital cameras and other devices.

The 1988 article lauded flash ICs with 4-kbit density. Today, devices with 8-Gbit density and more are commonplace. Alas, the semiconductor world is still looking for the perfect memory—one that offers the performance and price of DRAM and the nonvolatile nature of flash. Perhaps MRAM or some other disruptive technology will find commercial success in the future. EDN

10.27.88

FROM THE VAULT

## Conventional EEPROMs and flash EEPROMs offer a spectrum of bit densities



**Applications abound for nonvolatile-memory devices capable of occasional reprogramming. The storage of frequently used numbers in telephone equipment, password entry in security systems, patient-data monitoring in medical equipment, setup operators in word processors and printers, and mission-configuration parameters in military countermeasure equipment are just a few that come immediately to mind.**

**Although UV EPROMs meet the requirements of these applications, you have to remove them from the system before you can reprogram them. Theoretically, you could overcome this limitation by designing-in a large number of DIP switches, but this approach has practical drawbacks—imagine trying to include 2000 DIP switches in your design! EEPROMs offer a feasible alternative.**

**Nowadays, EEPROMs come in two guises. The flash EEPROM uses hot electrons to charge the floating gate. Manufacturers are still searching for a term to distinguish the flash EEPROM from its forerunner, a device that charges the floating gate through Fowler-Nordheim tunneling. The term most often bandied about is the full-featured EEPROM.**

**Because tunneling requires much less current for programming, manufacturers include charge pumps on full-featured-EEPROM chips to develop the high programming voltage from a standard 5V input. In addition, the requirement of a select gate allows the tunneling device to be programmed on a byte-by-byte basis. These two features are not currently available on flash EEPROMs.**

***Read the rest of this article at www.edn.com/article/CA6371935. For more Milestones That Mattered, visit www.edn.com/50th.***

**—by John A Gallant, Associate Editor, Oct 27, 1988**

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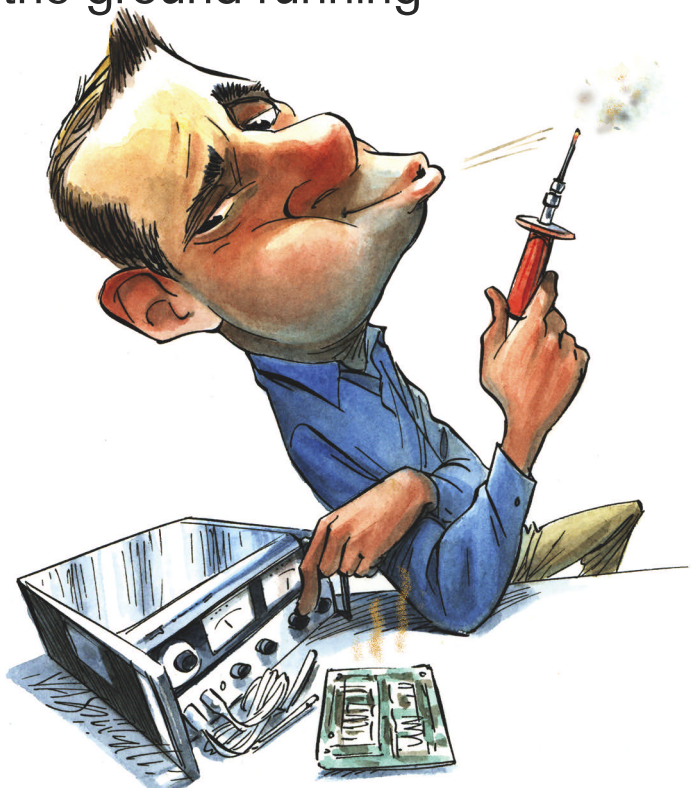

DANIEL VASCONCELLOS

My workbench includes a Hewlett-Packard 8405A VVM (vector voltmeter) of 1960s vintage. The VVM can convert two inputs at frequencies of 1 MHz to 1 GHz to outputs of 20 kHz, complete with modulation and sideband components. It can read signal levels as low as −70 dBm at full-scale and phase-difference readings over a range of 360° with 1.5° accuracy. With an APC (automatic-phase-control) PLL, it locks to the input-signal frequency in 10 msec. You can then measure level and phase angle in the presence of interference as high as −40 dBm and a signal level of −60 dBm.

Measurements of samples of the input signal with 300-psec pulses at a rate of 0.98 to 2 MHz produce the 20-kHz IF output. Such a pulse generator requires large, short, stable current-pulse outputs from the power supply, and even a small inductance can cause instability. The "APC unlocked; check signal/frequency range" front-panel indicator warns that the signal level or the frequency is out of the instrument range or that something is preventing the APC from locking onto the input signal. While I was using the instrument, this indicator came on.

Something in the unit had degenerated. So, I measured every waveform and voltage that could pertain to the PLL. The waveforms in the phase comparator, which resided nowhere near the pulse generator, were unstable, but there was nothing wrong on the pc board. I had changed transistors, bypassed and changed capacitors, and checked every voltage with the voltmeter and scope. I also sought trace breaks on the pc board and found nothing wrong with them. But the PLL *still didn't lock*!

The 300-psec sample-pulse generator resides on a pc board in a shield cage with sliding clips along the sides to contact the ground plane, and it has four edge-contact pins wired to the chassis. The ground wires were less than an inch long. Clearly, the HP designers knew that this circuit needed a good ground. Assume a ground wire ¾ in. (approximately 2 cm) long for a pc board with the pulse generator. The output is 300 psec—that is, $3\times10^{-10}$ sec wide. Such an output has energy at 3 GHz. The 2-cm ground wire has approximately 20 nH of inductance, or just about 400Ω reactance at 3 GHz. That ground is not a good one; that's why HP's designers used sliding clips and multiple ground wires.

The ground wires were intact according to the ohmmeter, but, with a circuit like this one, that criterion is not final. You can get the best assurance of adequacy by duplicating the ground connections at the pulse-generator edge connector. So, I connected four more wires, each more than 1 in. long, to a solder lug on the chassis and to the pc-board edge-connector ground pins. Now, the ground arrangement included the sliding clips along the pc-board sides; four wires, each less than 1 in. long, to a ground lug; and four more wires, each more than 1 in. long, to another ground lug—resulting in a circuit with eight wires in parallel!

Even for 3-GHz energy components, this arrangement should provide an adequate ground, and it did. The APC locked immediately. Now that the ground was good enough, the instrument worked correctly. The rivets holding the pc-board sliding clips to the aluminum chassis must have corroded over the years, causing more resistance. Perhaps the same situation was true of the ground-lug fastener that made the edge-contact ground connections. EDN

***Walter Lindenbach is a retired engineer. He lives in Calgary, AB, Canada.***

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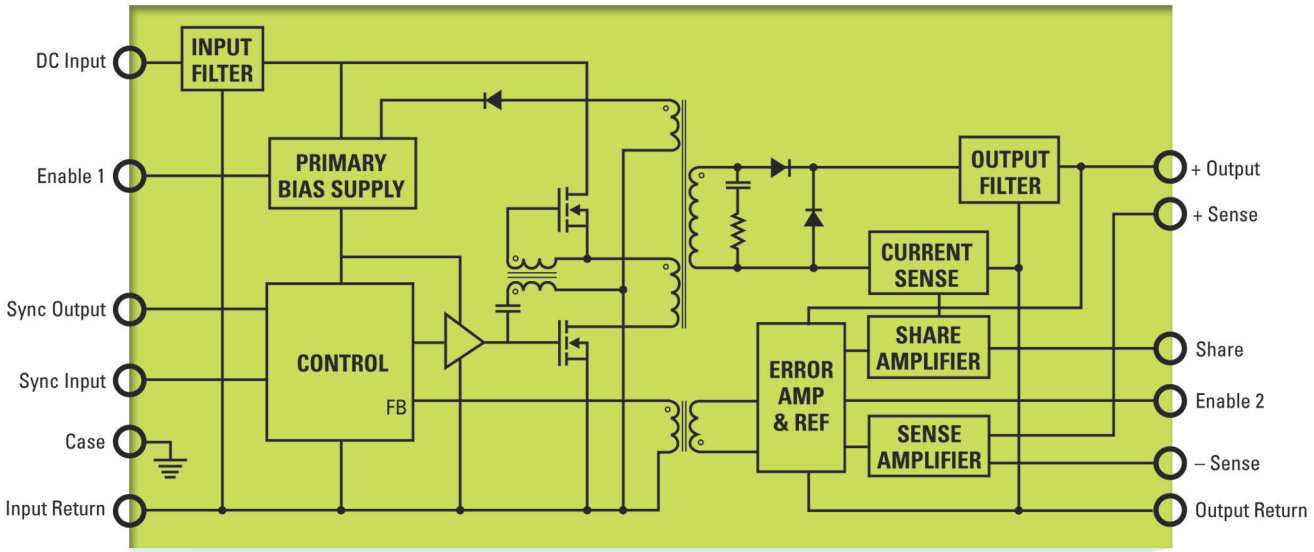
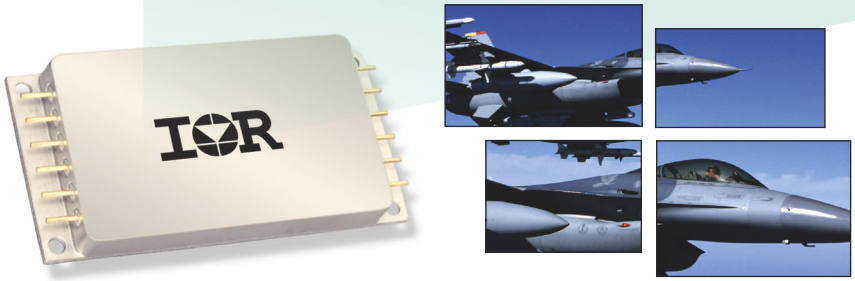
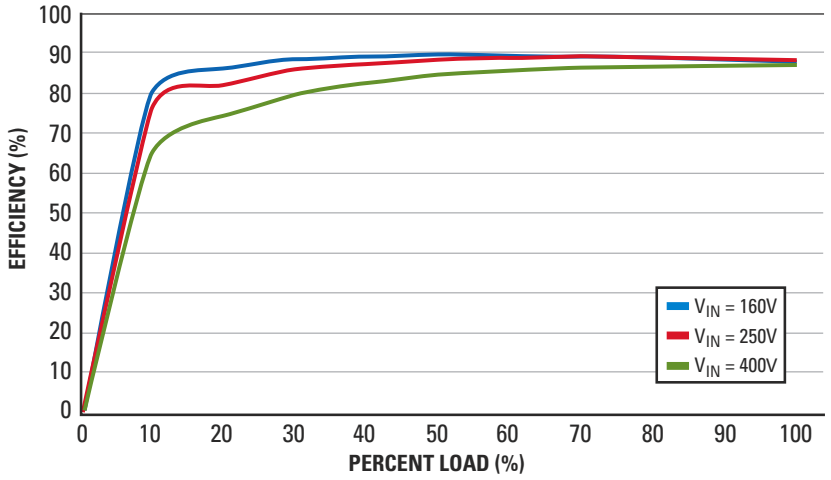



**AHP27015S: Efficiency Plot @ $V_{IN}$ = 160V, 250V and 400V, 25°C**

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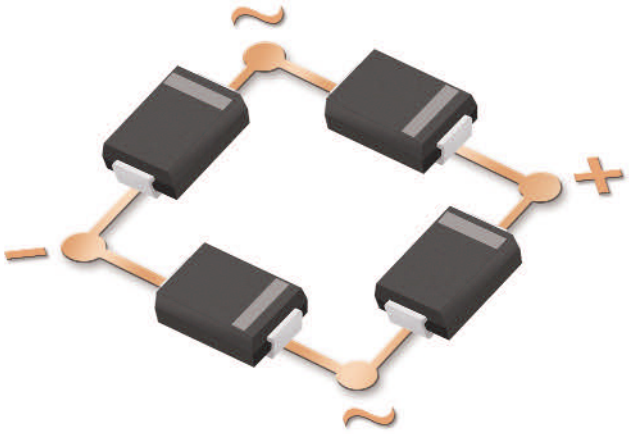

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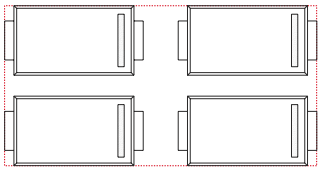
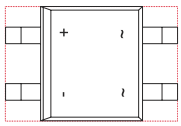


4 SMA packages



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ALTHOUGH ARM ARCHITECTURES INCREASINGLY VIE FOR AUTOMOTIVE AND INDUSTRIAL DOMINANCE, THEY FACE STIFF COMPETITION FROM PROPRIETARY DEVICES THAT REGARD THESE MARKETS AS THEIR OWN. RECENT DEVICES FROM MAJOR VENDORS UNDERLINE THE CONTINUING DETERMINATION TO COMPETE FOR MARKET SHARE.

BY DAVID MARSH • CONTRIBUTING TECHNICAL EDITOR

# PROPRIETARY ARCHITECTURES DEFEND AUTOMOTIVE SEGMENT

As *EDN Europe* reported in its December 2005 and February 2006 issues, the ARM architecture is enjoying increasing acceptance within the automotive and industrial markets that are traditionally the domain of proprietary designs (**references 1** and **2**). The recent announcement of ARM's Cortex-M—available for the first time in Luminary Micro's Stellaris family—strengthens this architecture's challenge by implementing a redesign that addresses comparative weaknesses in the original ARM7TDMI and its upwardly compatible successors, notably within real-time-response performance.

Unsurprisingly, vendors with long histories in the automotive sector are reluctant to cede market share and continue to introduce new silicon that raises the price and performance bar for application-specific devices. Several recent 32-bit proprietary products suit applications from general-purpose embedded control to infotainment, hard real time, and DSP, from the perspective of the low-cost-development environments that their makers believe will highlight each chip's capabilities.

In its previous Motorola Semiconductor guise, Freescale was among the first silicon makers to target the automotive sector. One of its most successful products—the PowerPC family, with devices such as the MPC565—enjoys widespread acceptance within the engine-management and power-train-control segments. The company's product portfolio also includes the ColdFire series of 32-bit machines, many of which enjoy success within industrial-control networks. Widening the application focus, the recent MCF5251 targets

portable and in-vehicle audio players, with interfaces for ATA-66 hard disks, a CD-ROM codec, SmartMedia, USB-On-the-Go, and serial-digital audio. Its V2 68K/ColdFire core includes an enhanced MAC (multiply-accumulate) unit with hardware division, which helps decompress streaming multimedia, making discrete DSPs unnecessary in many applications. The chip integrates 128 kbytes of SRAM and an 8-kbyte instruction cache, together with a system-bus controller and SDRAM interface to support the external-memory system. A ROM boot loader allows the chip to boot from hard-disk, $I^2C$, or SPI-connected devices. Two CAN (controller-area-network) ports augment the normal complement of microcontroller peripherals, and JTAG and BDM (background-debug-mode) interfaces ease system development. The budgetary price is $10.83 (1000).

The $949.50 M5251EVBWR evaluation system contains an M5251C3 single-board computer, a 2.2-in. TFT (thin-film-transistor) display module, a serial cable, and a universal power supply. In addition, a binder houses a 30-day evaluation copy of Wind River's Workbench on-chip-debugging-edition software, together with a Wind River Probe USB emulator that links the PC host to the board. Workbench provides all of the normal debugging and flash-programming features and is OS-aware for environments including Linux, ThreadX, and VxWorks. The software runs on Linux, Solaris, and Windows hosts. Presumably because this kit is so new, there's no board-support information in the package; you download it from Freescale's Web site. However, licensing issues mean that you must obtain authorization to download the Trio software for use with Workbench. There are no MCF5251-specific examples on the CD, but the MCF5251 home page carries software libraries with routines such as a graphic equalizer, JPEG video, MPEG-2 AAC (advanced audio coding), and MP3 decoders. There's also a binary image that's useful for proving that the flash programming system is operational.

The documentation reveals that the board carries 2 Mbytes of flash, 256 kbytes of which comprise the dBug monitor/debugger firmware that enables stand-alone operation with an RS-232 terminal. Or, that's the theory; our board resolutely refused to communicate over this port, simply sending error-break and break signals before locking up. Installing the Wind River software went seamlessly but did not create the HddSoftware examples directory that the printed booklet uses to introduce the system. Attaching the Wind River Probe worked fine, providing access to the microcontroller's on-chip JTAG-based debugging system at speeds that the company says are typically three to 10 times faster than competing products. The Trio software comprises a full application for an MP3 player—which requires an external ATA hard disk—but there are few pointers about how to get started within this complex environment. Freescale and Wind River are still working to improve the out-of-the-box experience, so if you're considering this evaluation platform, be sure to contact these companies for the most up-to-date support material. Wind River is currently offering a price incentive for customers who purchase this kit. For $5000, the software bundle comprises perpetual-seat, node-locked versions of the Compiler and Workbench suites and ColdFire-family support for the emulator that comes with the kit.

Another recent introduction from Freescale also demonstrates the ColdFire architecture and comes with the ubiquitous CodeWarrior environment, which is familiar to virtually every Freescale user. For $349, the M5208EVB evaluation kit consists of an evaluation board from Intec Automation, P&E Micro's USB MultiLink BDM interface, all necessary cables, and a power supply. The board's MCF5208, which costs $7.22 (1000), shares the same core and general-purpose peripherals as the 5251 but lacks the multimedia interfaces and the CAN ports; for industrial-network use, the 5208 adds a fast Ethernet port. Together with CodeWarrior, the software resources comprise a getting-started CD and Intec Automation's SBCTools board-support package for the µClinux (microcontroller Linux, pronounced "you see Linux") OS. There's also evaluation software from CMX Systems, Green Hills, MQX Embedded, and Treck. A 2-Mbyte flash device carries the dBug monitor together with the µClinux kernel, which facilitates a Web-browser interface, and a 32-Mbyte SDRAM provides program space. Interfaces include

**AT A GLANCE**

- Proprietary architectures fight to preserve market share.
- Accessible development environments are keys to success.
- The µClinux (microcontroller-Linux) OS speeds application-program development.
- Multicore processors tackle hard real-time control.
- DSP engines and software showcase real-time development.

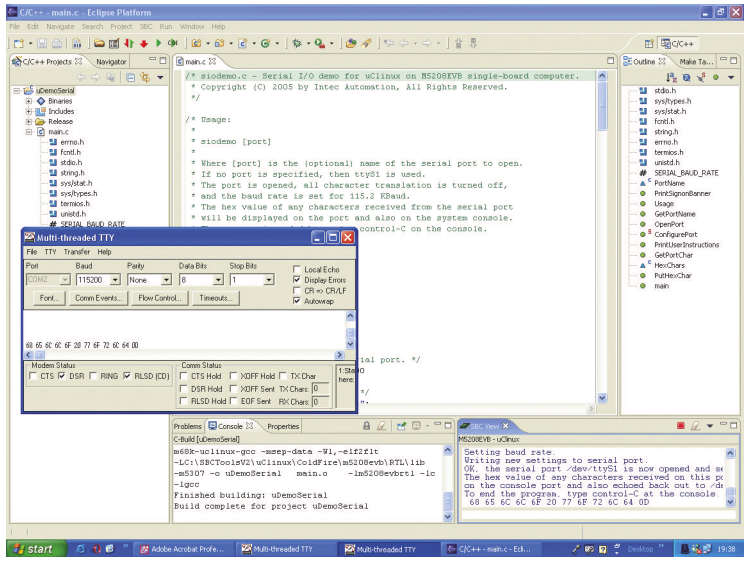


Figure 1 The µClinux kernel permits rapid application-program development using the M5208EVB.

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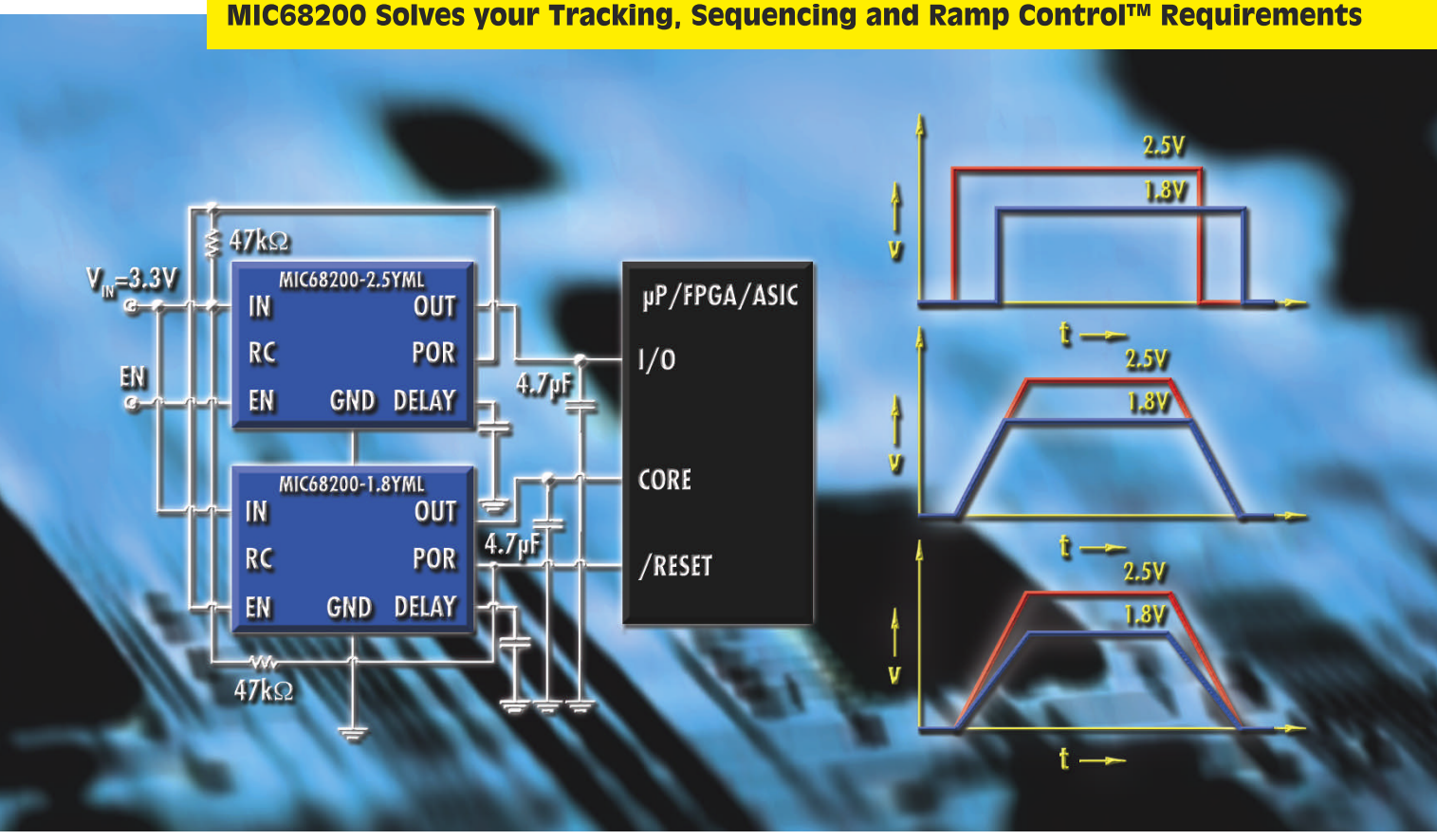


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serial and Ethernet ports, a BDM header, and a 16-pin header that makes available a range of signals including I²C and SPI buses. Echoing Freescale's presence in the ZigBee marketplace, the board features a ZigBee transceiver with a pc-board-track antenna.

The getting-started CD automatically runs a routine that scans the board and establishes serial communications with a terminal program at 115,200 baud, booting into μClinux. Providing that you reset your terminal program from this rate to 19,200 baud, removing jumper JP3 and rebooting displays the dBug-monitor prompt. A 54-pg manual describes the monitor's utilities, which include assembly/disassembly and flash programming, all of which are great fun for machine-code fans wishing to handcraft smaller projects. The abort pushbutton is especially useful here, as it generates a Level 7 interrupt that passes control from user code to dBug and preserves the machine's state. This action also automatically displays the ColdFire's core-register states. In case of accidental flash erasure, images of dBug and μClinux appear on the M5208EVB's Web page.

Larger projects will benefit from CodeWarrior, which the kit delivers in a 128-kbyte, code-limited special-edition format. With features such as Stationery providing templates that generate start-up scripts, the IDE (integrated development environment) provides support for assembler and C using the P&E hardware debugger. Helpful features include the USB-hardware-test routine, which confirms the probe's ability to force the 5208 into BDM, showing that the hardware is good. You can then rebuild CodeWarrior's example "hello-world" project for the BDM probe and run it on the evaluation board to verify the entire installation. Useful as a template for further development is an example program in CodeWarrior's installation directory that shows how to use the timer and general-purpose I/O to toggle the board's four LEDs. CodeWarrior-licensing options are available to add features such as instruction-set simulation, RTOS support, and Abatron's high-speed JTAG/BDM interface. The standard edition costs $2495, and the $5995 professional-version software supports the entire ColdFire family.

The SBCTools board-support-package CD installs the company's standard edition for use with dBug together with μClinux, Eclipse edition, which helps developers keen to try this increasingly popular kernel. The Eclipse environment entertainingly describes itself as "an open extensible IDE for anything and nothing in particular," yet it contains a full-blown C/C++ compiler and debugger, enough tutorial material to be genuinely useful, and utilities to share a Samba filing system and configure IP (Internet Protocol) addresses. However, getting the system to work was a struggle, starting with the TCP/IP (Transfer Control Protocol/IP) communications and culminating with the Samba file structure. The Ethernet issues took some experimentation to fix, but there's an obscure instruction in Version 2.0.0 of the user manual that claims it's essential to have a shared directory with the name SBCToolsWS for Samba to work. This statement is simply wrong: The environment doggedly directs itself to the default work-space directory and appears to ignore switch-work-space commands; hence, it never loads the object file from SBCToolsWS. So, obey the quick-start instructions and don't stray out of work space!

Even with a successful building and

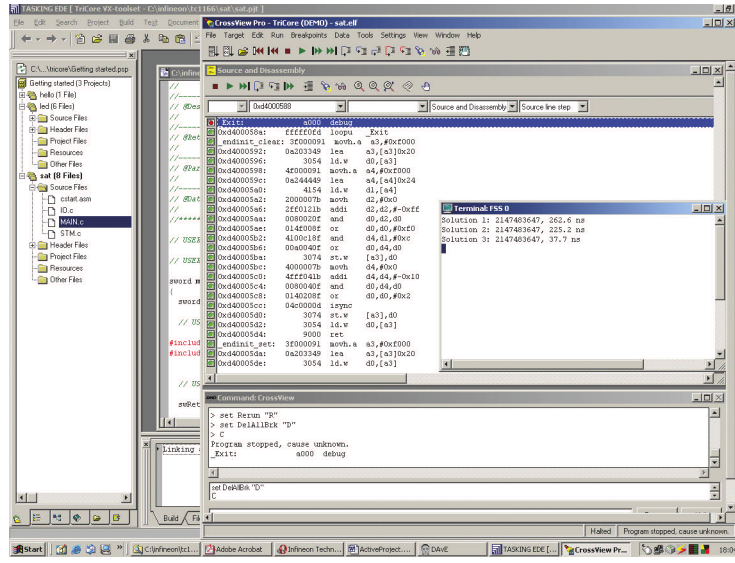

Figure 2 Language extensions within Tasking's compiler slash execution times for TriCore arithmetic.

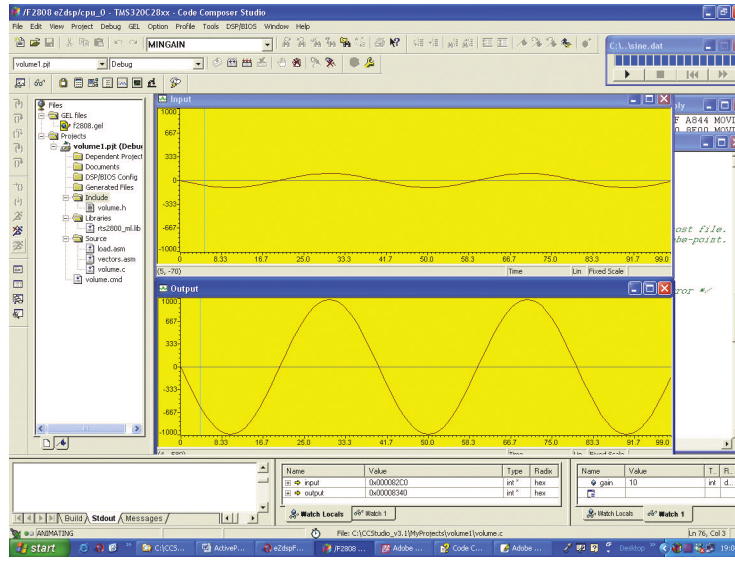

Figure 3 Code Composer Studio imports and processes data files from a PC host.

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| **DAC121S101** | 12-bit | 1 | 8 µsec | SOT-6, MSOP-8 |
| **DAC082S085** | 8-bit | 2 | 3 µsec | MSOP-10, LLP-10 |
| **DAC102S085** | 10-bit | 2 | 4.5 µsec | MSOP-10, LLP-10 |
| **DAC122S085** | 12-bit | 2 | 6 µsec | MSOP-10, LLP-10 |
| **DAC084S085** | 8-bit | 4 | 3 µsec | MSOP-10, LLP-10 |
| **DAC104S085** | 10-bit | 4 | 4.5 µsec | MSOP-10, LLP-10 |
| **DAC124S085** | 12-bit | 4 | 6 µsec | MSOP-10, LLP-10 |

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download, arcane error messages appear that state, for instance, "can't get /etc/mtab~ lock filesmbmnt failed: 1," which is confusing at the best of times. Help from Intec Automation's programmer, Mike Lavender, yielded a running serial-I/O sample program (**Figure 1**). From this point, it's easy to explore the facilities that the Eclipse environment offers, such as the tight integration between the GCC (GNU C compiler) and GDB (GNU debugger) that unusually run under Windows without needing the Cygwin Windows/Linux interface. The GDBServer implementation runs a version of the GDB on a PC host with communications through the fast-Ethernet port. Lavender notes that the executable file is "flat" with no file-name extensions: "This format allows the program to be placed anywhere in RAM when it is run as opposed to linking static addresses directly in the code. This allows the OS to run a program and even run multiple instances of the same program!"

If μClinux is your prime interest, see www.uclinux.org for news and developments for the many platforms that the OS supports, including ColdFire. Targeting microcontrollers that lack memory-management units, several μClinux projects are now maturing, such as the Analog Devices' Blackfin port, which uses the company's Stamp board (**Reference 3**). Also, don't forget Freescale's own ARM9-derived i.MXL Litekit, which *EDN Europe* reviewed last February (**Reference 2**). This multimedia-focused kit offers a particularly smooth introduction to Microcross GX-Linux, a port of the full Linux system.

## HARD-REAL-TIME FOCUS

Designed from the ground up to satisfy the hard-real-time needs of the automotive industry, Infineon's TriCore is one of today's newer architectures. A recent addition to the family, the TC1796, is a 150-MHz evolution of the TC1775, which the company introduced in 2000. As well as increasing the clock rate from the original chip's 40 MHz, this updated device carries 2 Mbytes of error-code-correcting flash, thereby addressing the TC1775B's principal disadvantage compared with its competitors. Other on-chip memory includes 128 kbytes of data flash that can emulate 16-kbyte segments of EEPROM, 192 kbytes of SRAM, and a

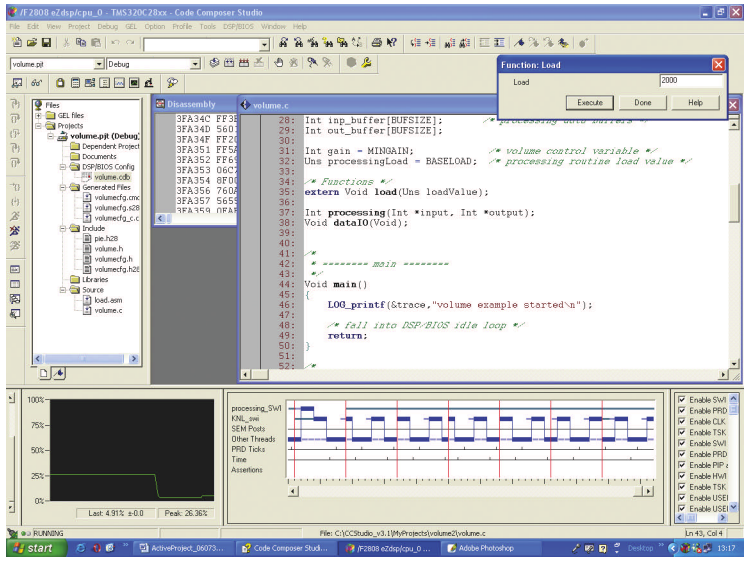


Figure 4 Automatic code instrumentation allows CCStudio to verify that routines meet real-time deadlines.

16-kbyte instruction cache. The TriCore nomenclature comes from the core's combination of a 32-bit, superscalar CPU; a single-precision, floating-point unit; and a DSP engine that exploits the best features of RISC, CISC, and DSP architectures. Separate program and data buses decouple the memory system from a range of I/O devices, each of which is optimized for flexibility and autonomous operation. The TC1796 also includes a 32-bit PCP (peripheral-control processor) that can autonomously handle I/O operations. The guide price for the TC1796 is approximately $27 (1000).

For about $400, Infineon's starter kit for the TC1796 consists of a Eurocard-format board; parallel-port cable; and software resources, including Infineon's starter-kit disk, an evaluation copy of Tasking's TriCore-VX tool set, and a board-support package from Hitex. Three more CDs contain sample development environments from HighTec, Lauterbach, and PLS. A getting-started booklet and a breakout board that brings the processor's I/O out to 0.1-in. headers complete the package. The kit requires an external ac or dc adapter that supplies 5.5 to 60V for the onboard power supply, which uses Infineon's TLE6389 buck converter to derive a master 5V rail with Texas Instruments' TPS76801 linear regulators downconverting to the 3.3V and 2.5V rails that the CPU's core requires. The board's major components comprise the SAK-TC1796-256F150E processor, 4 Mbytes of burst-mode flash, 1 Mbyte of asynchronous SRAM, and the usual array of I/O and switches. Most I/O connects to four high-density connectors, which is the reason that the breakout board is essential. The serial- and parallel-port interfaces have standard full-sized connectors, and the CAN interfaces come out to 0.1-in. headers.

The starter-kit CD's QuickStart subdirectory contains a step-by-step guide to installing and running the Tasking tool set and the Hitex HiTop debugger that form the default environment for this kit, as well as various code samples. To summarize a long story, the out-of-the-box experience did not go well. At first, the code examples failed to compile, which was due to the fact that the version of the Tasking compiler that came with the kit differs from the version used to develop the examples. It's an ongoing mystery about why Tasking's developers continue to think that it's acceptable to produce tools that cannot tolerate forward or backward compatibility, which has been a problem since the earliest days of the TriCore (**Reference 4**). After I fixed the compilation problems, several of the promising-looking hands-on training exercises failed to run. Investigation revealed that the initial training exercise leaves the TriCore's program counter pointing at the default blinking-LED routine in flash; hence, downloaded programs will never run. There were also some obscure board-to-PC commu-


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nication problems that required workarounds, all of which convey the impression that no one has properly tested this kit. But don't let any of this information dissuade you from considering the TC1796, which is clearly capable of outstanding performance (see **sidebar** "Generic platform speeds ECU development"). Furthermore, there are heavy hints that Infineon is working to resolve these issues; a capable software engineer can probably also accomplish this task.

Hearing of these problems prompted Infineon to donate a starter kit for the new TC116x series, which the company recommends as a simpler introduction to the TriCore family. Aiming at deeply embedded industrial-control applications, the TC116x family makes available a full complement of peripherals, including the Micro Link interface for interprocessor communication and the Micro Second bus interface, which provides high-speed control of external power ICs. The major operational differences between this 176-pin LQFP and the full-blown TC1796 are the absence of an external memory bus and the PCP. The roughly $295 starter kit comprises a Eurocard-format board whose processor's

## GENERIC PLATFORM SPEEDS ECU DEVELOPMENT

**Until recently, engineers wishing to develop new engine-management and power-train-control ECUs (electronic-control units) had to build custom electronics to interface with sensors and control critical processes, such as combustion. With the introduction of Infineon's PSK (power-train starter kit), it's now possible to employ a generic platform that promises to slash development times and standardize the hardware architecture–all of which have great potential for OEMs needing to minimize development costs and shorten time to market.**

**The platform leaves the software content with the developer, allowing OEMs to differentiate their products and retain their intellectual property. Interestingly, this goal wasn't Infineon's prime intention in developing the product, as Simon Brewerton, principal engineer at the company's UK development center, explains: "We wanted to be able to demonstrate our hardware to engine developers, but, as a silicon vendor, we don't possess our own engines and dynos [dynamometers]. It therefore made sense to work with someone who does to develop a general-purpose platform that's capable of controlling pretty much any engine, as well as being able to run a simulation mode for demonstration and training purposes."**

**The partner that Infineon chose is BigStuff3, a Michigan-based consulting company that specializes in designing aftermarket fuel-injection and ignition controllers for applications such as drag racing. The result is Infineon's PSK, which BigStuff3 also markets as the Gen4 development system. The kit comprises an environmentally sealed enclosure that houses the electronics and a generic wiring harness with standard connectors to mate with common engine and power-train components. The system controls as many as 12 fuel injectors and eight ignition coils, accepting inputs from as many as four inductive or Hall-effect camphase sensors, four Lambda sensors, and four knock sensors. It supports electronic throttle control and can control a five-speed torque-converter-based automatic transmission. Various ancillary outputs cater to devices such as fans and pumps.**

**A single pc board carries Infineon's TC1796 TriCore processor, which processes analog and digital inputs from an array of sensors and drives power-stage outputs built from a combination of the company's protected MOSFET power switches (Figure A). The hardware architecture is deceptively simple but extremely powerful, showcasing the TriCore's real-time computational prowess and the power of its peripheral-control processor to perform every necessary action in real time. Brewerton notes that the secondary XC164 processor acts as a check system for electronic throttle control: "In a real application, the XC164 handshakes data with the TriCore over an internal CAN [controller-area-network] bus, performing checksums and so on to ensure that everything is running properly. But, for training and other simulation purposes, it can also generate all the signals that the TriCore needs to simulate a running engine–effectively providing a 'virtual engine' for hardware-in-the-loop capability."**

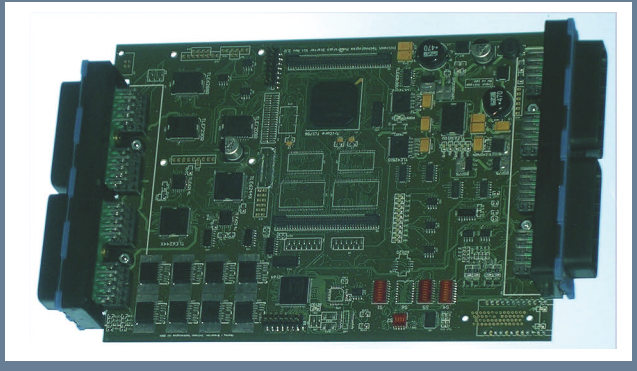

Figure A A single board carries the TriCore processor and all interface channels.

**Brewerton says that engine-control strategies comprise a mix of three major elements–state-machine control, look-up tables, and functional models–all of which endeavor to accurately estimate what's happening within the combustion chamber. For instance, flow-control models predict the basic physics of fuel-to-air-input ratios and quantities to exhaust-gas output. As ever, the better the control accuracy, the better the end result–which, in this case, is the maximum power output for minimum fuel consumption and pollution; pollution control is today's prime driver of ECU development. Engine position is a princi-**

identifier has been blanked out; a note says that it's a superset of the TC1166, a standard chip that costs approximately $14 (1000)—along with the power supply, an RS-232 port, and a parallel port to drive the JTAG interface. You also get a short plug-to-plug parallel-port cable, a breakout board to access I/O lines, a universal-input power supply, and a starter-kit CD.

The February 2006-dated CD contains a getting-started guide, the TriCore manuals, and software that includes Infineon's excellent chip-configuration code-generator DAVE (Digital Application Virtual Engineer) Version 2.1r22. Apart from its primary role in initializing the processor, DAVE is a tool that rewards investigation, as its layers reveal a great deal of useful information about the target chip, which can be any TriCore or 166-family device. The tool's output is a fully documented, free file that you can import straight into a project. The default compiler is Version 2.3r1 of Tasking's environment, which the kit couples with the UDE (universal-development environment) from PLS. There are samplers of HighTec's GNU-based development environment and Lauterbach's

**pal control input, with the main angular input typically deriving from a 58-tooth crankshaft position sensor (actually, 60 with two missing) on the flywheel. From this timing input, the control system derives angular information with 6° of native resolution.**

**A typical PSK application uses the TriCore's GPTA (general-purpose timer array) to debounce camshaft- and crankshaft-position sensors before using the flywheel input to run a PLL (phase-locked-loop) at 2048 times gear-tooth speed, thereby increasing angular resolution to 0.0029° per pulse. As the PLL locks to the incoming frequency, software can assess changes over time that signify events such as acceleration and make appropriate adjustments–including compensating for undesirable effects, such as the torsional resonances that peak when the furthermost cylinder from the flywheel fires in an inline engine.**

**Another key control input comes from piezoelectric resonance sensors on the cylinder head that detect "knock," or pre-ignition. These sensors are tuned to the block's resonant knock frequency, which typically lies within 8 to 12 kHz. Brewerton asserts, "The limit on engine performance is the onset of knock. As every 1° of ignition advance approximates a 1% power gain, it's essential to run the engine as close to the limit as possible." One problem is that, when knock sets in, it can take many degrees of timing retardation to restore normal operation, so most manufacturers leave a guardband of 2 to 3° of retard to ensure that the engine does not pre-ignite. If you can detect the onset of knock early on, it's possible to reduce this value and increase power output.**

Figure B The TC1796ED emulation device has a USB port in the silicon.

**The TriCore includes a 3.5M-sample/sec ADC with autonomous trigger logic that can oversample as many as four knock-sensor channels before passing the data to the chip's DSP block. The block contains dual multiply-accumulate units that can generate two new results per clock cycle. As the trigger logic ensures the phase coherency of data capture, a fast-Fourier transform can extract the real signal and evaluate its energy content. Software can exploit this technique to create a frequency profile that significantly increases knock-detection sensitivity–also allowing a look-up table of maybe 128 entries to make the fine adjustments in engine-speed-dependent knock-center frequency. Another possibility for vibration profiling lies with predictive maintenance, such as detecting the onset of bearing failure.**

**The look-up tables that carry engine-calibration data are key components in any ECU and can run to several hundred kilobytes. It's essential for development engineers to be able to transparently modify calibration constants as the engine runs before locking down satisfactory values in nonvolatile memory. Traditionally, hardware tools access dual-port SRAM that overlays the flash calibration memory to facilitate dynamic changes, but a special emulation-device version of the TC1796 improves this process.**

**The TC1796ED carries on-chip emulation logic as well as 512 kbytes of SRAM that can act as a calibration overlay area, all connected to the outside world through a USB port on top of the chip (Figure B). This unique arrangement allows a calibration engineer direct access to the running under-hood hardware using nothing more than a laptop and some software. The emulation interface provides access to Nexus Level-III application-programming-interface features, allowing toolmakers such as ETAS to offer calibration tools based on a generic model. The SRAM is also capable of real-time data capture, allowing the interface to stream time-stamped data to tools from vendors such as Lauterbach and PLS that offer emulation tools with logic-analyzerlike functions for event reconstruction and tracing and code debugging.**

**Although the PSK targets spark-ignition engines, Brewerton reports that various customers have successfully adapted the system for diesel motors that range from passenger cars to giant earth movers. In these applications, the TriCore controls direct-injection sequences that typically require five to seven injection bursts per ignition cycle to minimize pollutant generation. The PSK is available now for approximately $3400 and comes with sample software projects; approximately $1500 more buys you a version that includes the TriCore-emulation device.**

Trace32 debugger, together with OS samplers from Enea and Euros. You also get a free copy of Infineon's TriLib DSP library for TriCore. The opening screen promises that you can be up and running within 30 minutes of unpacking the kit, which the screen assists by providing hyperlinks to install the Tasking compiler, the PLS debugging engine, and DAVE, which the program samples use.

Sadly, the first hello-world program failed to compile, generating more than 40 error messages before giving up. This problem—which the kit did not document—is due to an incorrect linker setting for TriCores without external memory, as a release-note entry on Tasking's Web site for its Version 2.3 compiler reports. Changing the linker-script file settings for internal memory so that SPRAM's (single-port RAM) Alloc attribute is on and its Type is ROM allows the six samples to compile and run correctly. These samples progress from hello world, which demonstrates studio support in an embedded environment through a blinking-LED I/O-port routine, to samples of handling arithmetic saturation, interrupts, serial I/O, and on-chip flash programming. The arithmetic sample shows the power of Tasking's C-language extensions, which map directly to TriCore instructions, slashing the sample code's computation time from 262.6 nsec for 32-bit ANSI-C to just 37.7 nsec for the 64-bit Tasking implementation (**Figure 2**).

One sample uses the timer array to generate a 1-sec interrupt that toggles the TriBoard's LED—in the meantime showing that the TriCore supports as many as 255 interrupt sources that can each have a unique priority level set from within DAVE. Although most processors load new program-counter values to run interrupt-service routines, the TriCore minimizes interrupt latency by jumping to vectors in code memory. The serial-output routine then builds on the IRQ (interrupt-request) exercise to output an updating message to HyperTerminal. The final example uses the UDE tool set from PLS to program the TC1166's flash with a variation of the serial-output routine. This method also works, providing that you set the tool to Infineon's DAS (device-access server) rather than the default starter-kit JTAG driver and power down or power up the TriBoard when programming completes.

Although all tool chains are subject to personal preferences, the most popular TriCore setup combines Tasking's compiler with the HiTop debugger from Hitex. But don't ignore the other possibilities; besides the choices that appear on the starter-kit CD, Infineon's Web site lists compiler choices that range from GNU freeware to approximately $3000 to $4000 for a commercial product with maintenance and support. Because Infineon uses a parallel-port "wiggler" interface, it's easy to duplicate the simple logic that appears in the schematics for use with your own prototype hardware. You can then use the tools that accompany this kit to perform basic hardware and software debugging at low cost. For "proper" development, the TriCore supports three levels of debugging through its on-chip-debugging system (**Reference 5**). Infineon reckons that the runtime control and internal access that Level 1 offers is sufficient for approximately 80% of applications. Level 2 adds instruction

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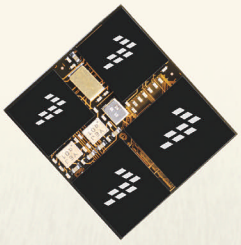

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IT'S HARD TO BEAT A DSP ENGINE WHEN IT COMES TO PERFORMING REPETITIVE COMPUTATIONS ON CHUNKS OF DATA IN REAL TIME.

tracing, and Level 3 is full-blown real-time in-circuit emulation that includes trigger logic, trace and overlay memories, and the ability to view the chip's internal buses. The budgetary range for these tools spans starter-kit prices through $5000 to $8000 for Level 2 facilities to approximately $10,000 for Level 3 capabilities.

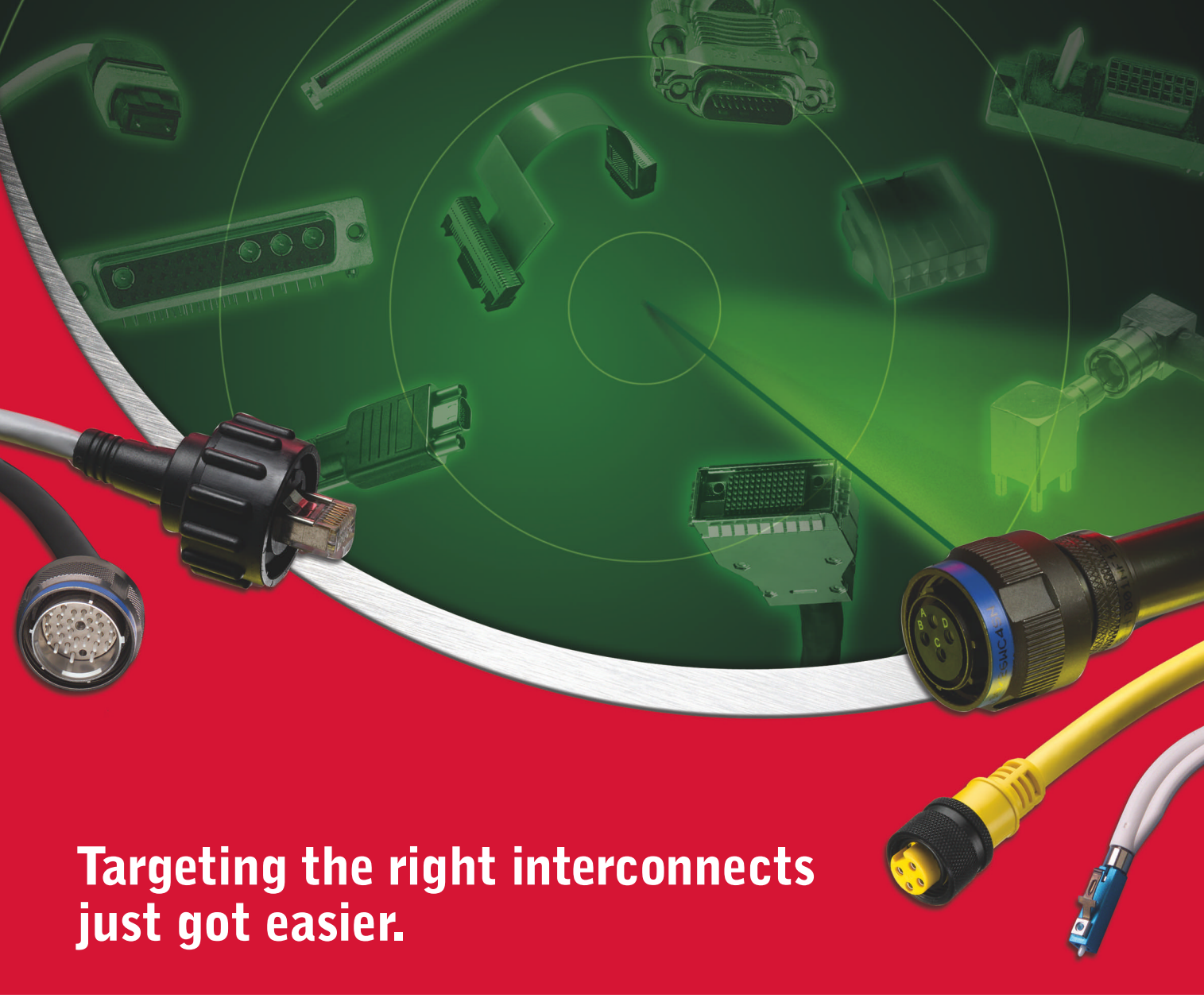
## DON'T DISMISS DSP

From audio decompression to vibration analysis, it's hard to beat a DSP engine when it comes to performing repetitive computations on chunks of data in real time. Yet, many engineers shy away from the technology, believing it to be too complex and expensive. However, with a budgetary guide price that starts at $11.60 (1000) for the 100-pin BGA package, the fixed-point TMS320F2808 from Texas Instruments lies at the low-cost end of the DSP spectrum. Targeting real-time control, the chip packs 36 kbytes of SARAM (single-access RAM) and 128 kbytes of flash alongside the 100-MHz C28x core, augmenting the normal complement of microcontroller peripherals with dual CAN ports and a 16-channel PWM module. It also has a 2-kbyte one-time-programmable ROM block and a separate 8-kbyte boot ROM. Crucially for real-time use, the chip features hardware debugging, which the accompanying CCStudio (Code Composer Studio) suite comprehensively exploits. Software support includes TI's DSP/BIOS kernel, as well as a number of libraries, such as high-speed fixed-point arithmetic routines and digital motor-control algorithms.

Spectrum Digital offers its $469 TMS320F2808 eZdsp system kit, which contains a compact development board, a resource CD, a USB cable, a power supply, and the obligatory getting-started flier. The board is home to the target 320F2808 DSP, an Actel FPGA, an MS320DA255 chip, two switch arrays, and various support logic, including serial-boot EEPROMs. Two nine-pin D connectors bring out the primary CAN and SCI buses, with secondary instances of each available on 0.1-in. headers. The final header supports an optional JTAG emulator, as the kit uses a USB connection for this purpose. Two unpopulated header layouts optionally allow you to connect general-purpose-I/O and analog signals, taking care to ensure that external-signal levels don't exceed the F2808's 3.3V I/O levels. To prevent the F2808 from latching up with possibly destructive effects, it's also necessary to power the eZdsp board before applying any external signals, so consider hot-pluggable level-translating transceivers for any custom interface that runs at normal automotive or industrial 5V levels.

Installing CCStudio together with the board-support package and a flash-burner utility completes seamlessly in about 10 minutes, when an XP Pro machine automatically installs the USB drivers, which you can test by launching a desktop diagnostic icon. In this case, the installation created icons for the F2812 version of CCStudio as well as the desired F2808 instance, but this aberration didn't affect the kit's behavior; however, it proved impossible to register CCStudio, as the service code was missing from the CD case. It transpires that the software that we received with our kit is the full Platinum version rather than the free-kit version, which similarly has no code-size limit.

The F2808 section of the downloads area at Spectrum Digital yields documents that include hardware-reference guides and schematics as well as the board's getting-started guide, which directs users to CCStudio's integral tutorial. This invaluable facility comprises three modules that introduce users to the IDE, the DSP/BIOS real-time kernel, and the real-time-emulation facilities. Nice touches abound. For example, the IDE automatically imports the appropriate "include" files for a project. You can also get help on an assembly-language instruction by clicking on it and hitting F1. But the IDE includes some truly slick features, such as the ability to import test-stimulus data from a PC file to the board and return result data using a



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**EFFECTIVELY A SPECIAL KIND OF BREAKPOINT, A PROBE POINT TEMPORARILY HALTS THE TARGET TO PERFORM THE DATA TRANSFER BEFORE AUTOMATICALLY RESTARTING THE PROCESSOR.**

probe-points mechanism for file I/O. Effectively a special kind of breakpoint, a probe point temporarily halts the target to perform the data transfer before automatically restarting the processor—a technique that suits program development rather than real-time verification. You can graph the result data by setting parameters under the View menu and animating the outputs for the sample sine-wave input data and a processing gain of 10 (**Figure 3**). Other key IDE features include a profiler that helps identify sections of code requiring optimization and the GEL (general-extension language), which allows you to automate CCStudio setups and perform runtime functions.

The DSP/BIOS kernel consists of a set of modules that you can link into an application to provide real-time scheduling, synchronization, and host/target communications. It employs code instrumentation to monitor program activity on the fly and automatically instruments any code that uses the kernel's pre-emptive-multithreading ability. A configuration tool links in only the DSP/BIOS objects that are necessary for the user's program and allows you to set up memory, interrupt handlers, and thread priorities. The tutorial first describes how to measure the cycle count of the stdio.h function "puts," which writes the inevitable hello-world message to the console. You should then be able to see how the DSP/BIOS-call log speeds I/O. In this case, this operation stalled, presumably due to a failure in the RTDX (real-time-data-exchange) subsystem, although the diagnostics report correct operation. By contrast, the next example that shows thread-execution measurements using the real-time-analysis functions within DSP/BIOS ran perfectly, thereby demonstrating the environment's ability to ensure that a process meets a deadline. You can demonstrate this situation more clearly by using the CPU load graph while testing the time line by adding dummy cycles using the load function from the GEL environment (**Figure 4**). Other DSP/BIOS tutorial topics include analyzing real-time behavior and connecting to virtual I/O devices, and there are thoughtful "things to try" throughout the material.

If all of these features aren't enough, there's a great deal more material available from TI's Web site, such as the free getting-started-with-DSP material that's so popular with students and engineers alike. (Also see *EDN Europe*'s coverage in **Reference 6**.) Automotive users may be particularly interested to see the eZdspF2808 diagnostics and demo-source-code Version 2 material that appears at Spectrum Digital's F2808 page. As well as source and project files for F2808 diagnostics, this code includes a CAN loop-back test program. Converts can purchase an annual license for the TMS2000-only version of CCStudio for $495, and the universal version, which permits development on any TMS320-family chip, costs $3595. **EDN**

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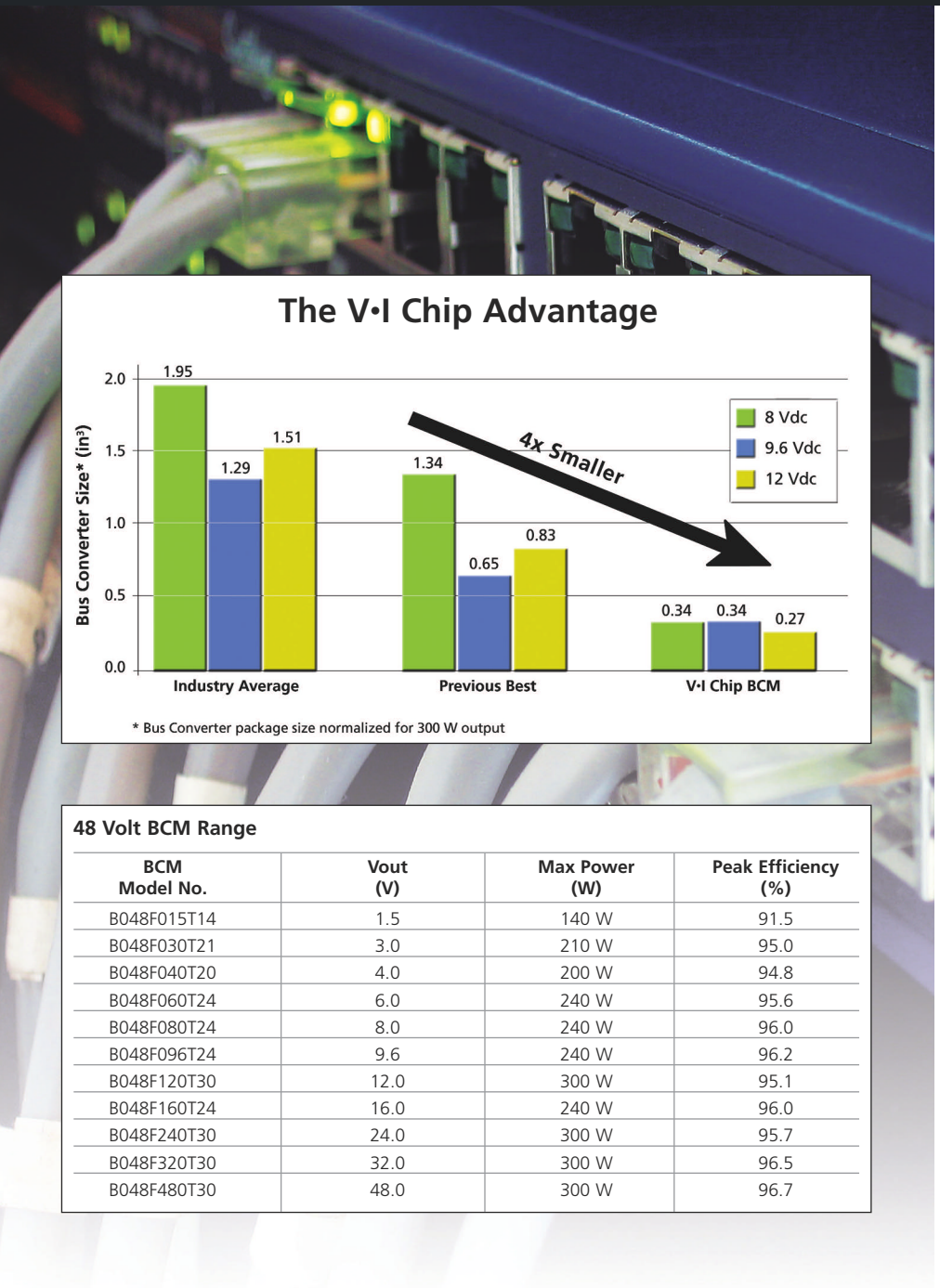

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POWER
FROM LINEAR TO DIGITAL

BY PAUL RAKO • TECHNICAL EDITOR

POWER—FROM LINEAR TO DIGITAL—COVERS A RANGE OF DESIGN CHOICES. THIS BRIEF OVERVIEW PRESENTS DESIGNERS WITH SOME OF THE ALTERNATIVES AND PROBLEMS THAT WILL ARISE.

# CREATING THE POWER SUBSYSTEM IN MODERN DESIGN

Power electronics range from the simplest to the most complex subsystems in modern products. This fact is not surprising because the applications also range from simple to complex. At the simplest, a power supply can be a big zener diode, such as those that find use in submarine cable-repeater pods. These pods need the ultimate in reliability, and a resistor-plus-diode approach is the simplest and hence most reliable. The zener dissipates a significant amount of heat, but the temperature of the ocean floor easily removes that heat. Slightly up the complexity ladder are linear regulators—popular and useful parts. The LM317

is the most frequently downloaded data sheet at National Semiconductor's Web site. A linear regulator operates like a valve. It resists the current in the circuit to ensure that voltage stays constant. Remember that the word "transistor" derives from the combination of the words "transconductance" and "varistor" (**Reference 1**). The transistor in a linear regulator pinches off the current to control voltage—hence, it provides transconductance. In this operation, it serves as a variable resistance, or varistor. Conventional linear regulators have NPN-pass elements. Low-dropout regulators use PNP transistors.

A more complex regulator is the charge pump. It uses several transistors as switches, not linear elements. These switches transfer charge to a capacitor and then change the connections so that the capacitor doubles or inverts the original voltage you impress upon it.

You realize a large jump in complexity when you move to switching regulators. These circuits have high-frequency magnetics, a control loop, and at least one transistor acting as a switch. You can buy the entire regulator as brick from Vicor or Tyco, or you can roll your own and build the regulator from parts. Buck, boost, inverting, isolated, SEPIC (single-ended primary-inductance converter), and Cuk (pronounced "chook") are all types of switching regulators.

All of these power circuits convert one dc voltage to another dc voltage. A significant number of designs use transformers to change ac voltage or circuits that convert ac to dc for subsequent dc-to-dc conversion. One of the most elegant ac-to-dc-conversion circuits, the PFC (power-factor-correction) circuit, uses a boost-converter topology to ensure that the input current to a converter is proportional to the input voltage, unlike the sharp spikes of input current that occur in conventional ac-to-dc circuits.

A new term in the power world is "digital power" (**Reference 2**). It can mean anything from simply being able to use a digital input to shut down the regulator, to having digital communication to the chip for monitoring and control of the analog-PWM process, to having a DSP close the loop and directly control the pass element with a PWM signal.

Starting with the basics, a linear regulator uses a transistor to step down a dc voltage. A conventional linear regulator, such as the LM317, uses an NPN transistor as the restriction. Because of the 0.6V drop in the base-emitter junction, these regulators need a significant amount of head room to operate. Engineers often mistakenly assume that the output voltage is in regulation even when the part is maintaining less than the recommended dropout voltage. The part may provide the right voltage but does not meet several ac and thermal specs. Engineers lived with the large head-room requirements of linear regulators until the early 1980s, when US automobile manufacturers approached the semiconductor industry with the need for a low-dropout linear regulator. The regulators designed for low head room, such as the LM2936, used PNP pass transistors. This approach allowed the regulated circuit to stay in regulation even if the battery voltage sagged to 8V during the car's cranking period while starting. According to Al Kelsch, product-definition manager at National Semiconductor, as the dropout voltage approached zero, a "caret," or small spike of input current, would arise because the base of the pass transistor was at maximum turn-on. Although the IC designer spent a lot of time designing a base-drive circuit that would limit the current and eliminate the caret and still provide transient response and other specs, customers needed that little caret to sense when the regulator dropped out; they could then turn off the entire circuit. In other words, customers viewed as a feature what the designer perceived as a bug.

The overriding problem with linear regulators is heat. Because the regulator has both significant voltage and significant current running though the pass transistor, it dissipates a lot of power. Most linear regulators have a thermal shutdown, which may save the part from destruction, but it also makes the circuit unusable if the shutdown happens in any operating situation.

Another design issue with linear regulators also applies to most power supplies. You must assume that any electrolytic capacitors will short-circuit at some point during the lifetime of a product. If a short circuit occurs, you must ensure that the regulator and board do not burn or cause other damage. You must also provide a fuse or a fusible pc trace on the input electrolytic capacitors and on any tantalum capacitors. Even if the product's wall wart cannot provide enough current

## AT A GLANCE

- Power subsystems can be linear, switching, charge pump, ac/dc, digitally managed, or digitally controlled.
- Linear supplies face thermal issues.
- Charge pumps entail noise injection.
- Switching supplies must deal with stability, noise, and thermal problems.
- Digitally managed and digitally controlled power often requires a software effort right before product release.

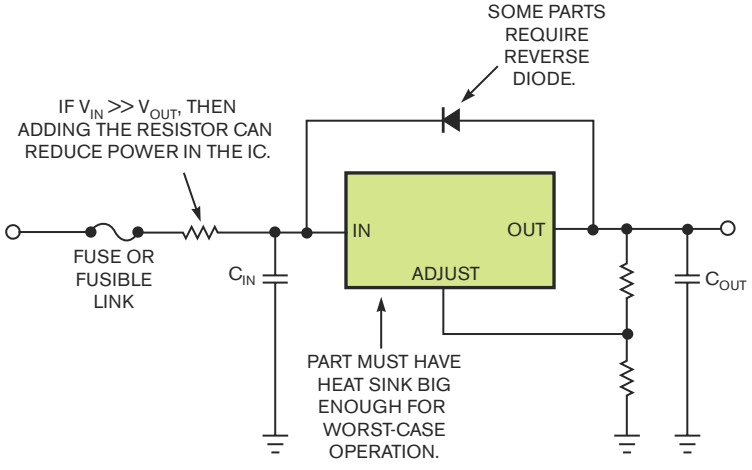
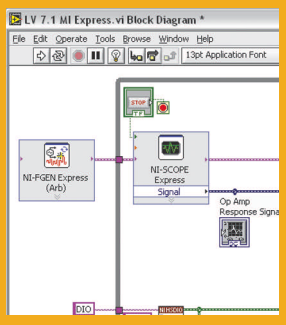
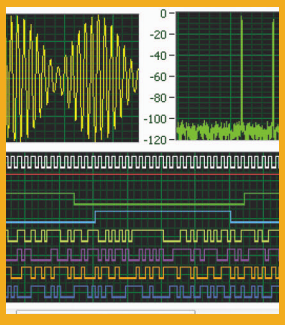
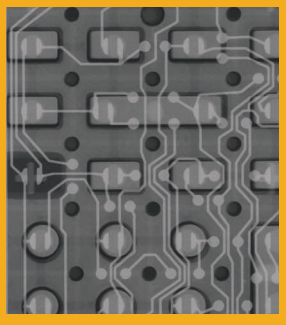
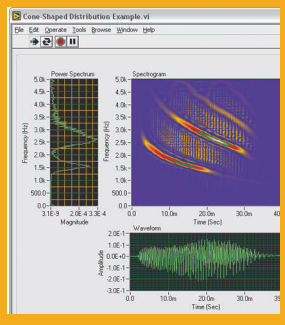


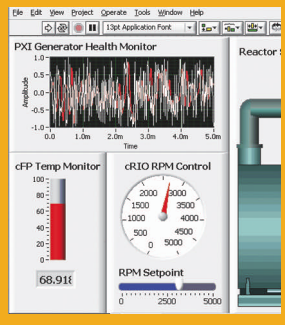

Figure 1 Linear supply problems are heat, capacitor shorting, and damage to the part when reverse currents flow inside the IC.

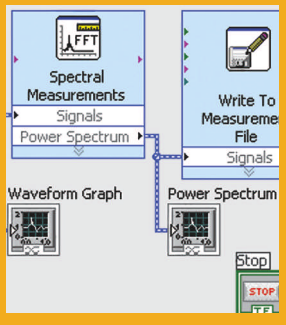







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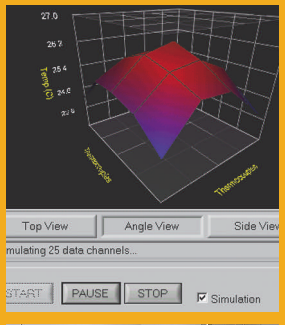



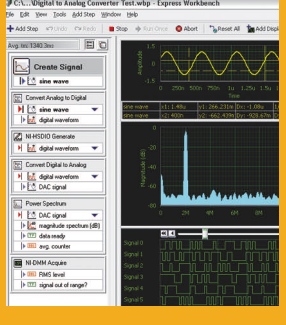

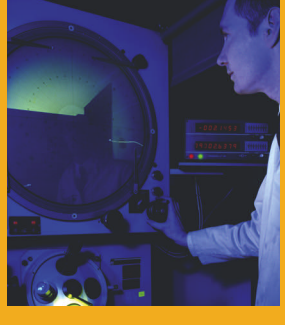
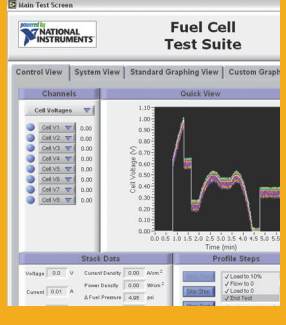

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to start a fire, a diligent engineer must provide for the situation in which a user uses a larger or incorrect wall wart to power a product (**Figure 1**).

## CHARGE PUMPS

Another type of dc/dc converter, the charge pump, can invert, double, or triple an input voltage by switching a capacitor across the input voltage to charge the capacitor. You can then switch that capacitor to sit on top of the input voltage, forming a doubler. Alternatively, you can connect the positive terminal of the capacitor to the input common, creating a voltage inverter. The classic charge pump is Intersil's ICL7660, which the company introduced in the 1980s. Another such device, Catalyst Semiconductor's CAT3636, employs a novel method of achieving noninteger voltage steps of 1, 1.33, 1.5, and 2V. This approach allows efficiency as high as 92% in handheld-system applications. This efficiency compares with that of conventional inductive boost converters, especially in view of the fact that many manufacturers specify efficiency numbers for those converters based on unreasonably large inductance.

Because the capacitor inherently limits the amount of current that the part can deliver, thermal problems are rare in charge pumps. They do have some drawbacks, however, including poor voltage regulation. The output changes with the input unless you employ a linear postregulator. Maxim has addressed this issue with a line of postregulator charge pumps. The switching frequency and noise of a charge pump are far less problematic than the noise from a switching converter, but the noise may still enter the signal chain.

Another type of regulator, the switching regulator, uses a transistor switch with an inductor or transformer to change a dc-input voltage. **Figure 2a** shows a buck-switching regulator that steps down a voltage and that operates analogously to a water wheel (**Figure 2b**). The device's rate of rotation is analogous to the current following through the inductor. Just like an inductor, the water wheel cannot instantaneously stop or start. The **figure** may give some insight about why engineers often refer to the diode as "freewheeling." When the valve turns off, the inertia of the water wheel creates a powerful suction. The wheel needs water to keep rotating, and the check valve provides this function.

A boost converter employs the same water-wheel analogy (**Figure 3**). Many engineers have trouble with magnetic circuits because their high reactance means that the current does not track the voltage as it does in a resistor. An intuitive understanding of the buck and boost converters allows you to understand the more complicated architectures, such as Cuk, boost-buck, and SEPIC. Converters can also use transformers to create an isolated output (**Figure 4**). Flyback converters, which differ from forward converters only in the polarity of the output diode, use a transformer as a choke. They store energy in the magnetic field when the switch is closed and as current increases in the primary. When the switch opens, the energy in the magnetic field discharges through the secondary. Designers favor flyback converters for their low cost and their ability to make multiple outputs that all track each other reasonably well.

Most engineers have difficulty designing robust switching converters. The first problem is stability. Stabilizing their complex control loops can be a daunting task because many converters require a ripple in the output voltage to work properly. Others exhibit subharmonic oscillations, and you must inject a ramp signal into the reference. When large-value ceramic capacitors became affordable, many engineers substituted them

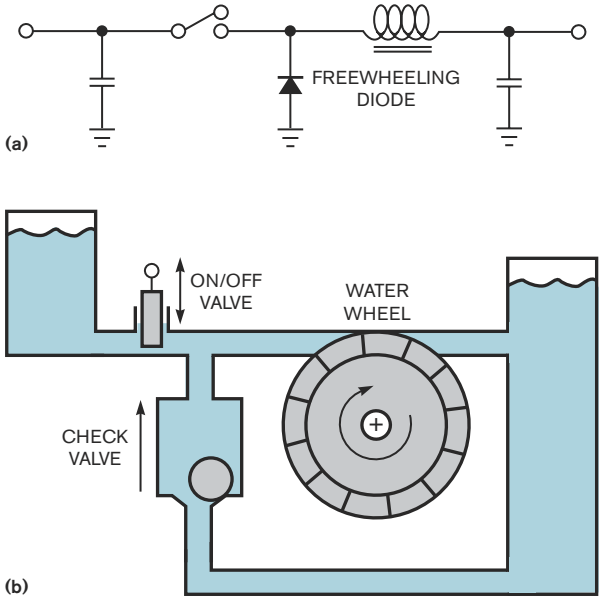


Figure 2 A buck regulator steps down the input voltage (a), and you can make a water-wheel equivalent (b).

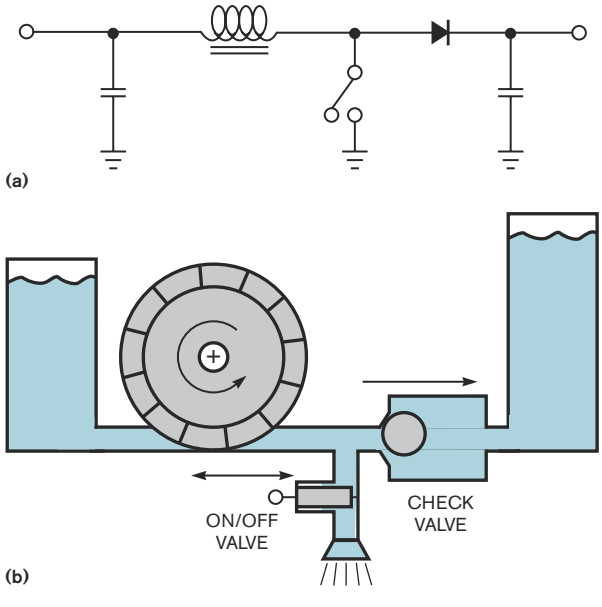


Figure 3 A boost regulator steps up its input voltage to a higher level (a), and a water-wheel equivalent provides insight to the circuit (b).

# Why settle for a slice?

# When you can have the whole pie...

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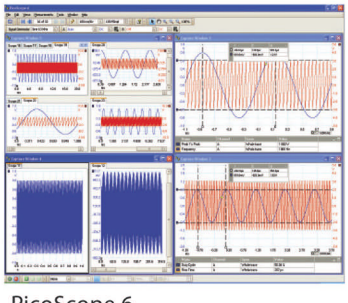

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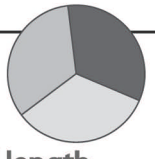

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Another common problem, noise, can radiate back into the input or output power lines or radiate into space as electromagnetic radiation. The worst issue with this problem is that a designer may not notice it until sending the product for FCC (Federal Communications Commission) and CE (Conformité Européenne) testing just before production. Designers can use various techniques to shield this noise from the world and the rest of the system. It is better to not generate the noise in the first place than to later attempt to shield it in tens or hundreds of end-user applications.

As with linear regulators, thermal issues can also be problems in switching converters. Most buck regulators generate more heat in the freewheeling diode than in the FET. A thermal plot from National Semiconductor's Webench online-design tool shows that diode $D_1$ is the hottest component on the board and is heating the IC it abuts (**Figure 5**). To reduce the heat that freewheeling diodes generate, synchronous buck regulators replace the diode with a second out-of-phase FET.

Most of the above problems are traceable to an inferior pc-board layout. Several articles are available that discuss the pitfalls of laying out a good switching regulator (**references 3** and **4**). Engineers should always take advantage of the applications-engineering staff of the companies that make the regulator IC. They can avoid an enormous amount of frustration and chaos if the applications engineers can review your design and layout before you commit the board to fabrication.

## OFFLINE REGULATORS

This article has so far discussed only dc/dc converters. Another class of converters creates dc power from ac power. The ac power most commonly comes from residential ac-power lines; the converters are thus offline supplies (**Reference 5**). Other designs use an isolated topology to create one or more dc supplies from raw dc power from the classic rectifier circuit. Allegro, On, STMicro, Power Integrations, and the Unitrode division of Texas Instruments make these types of devices.

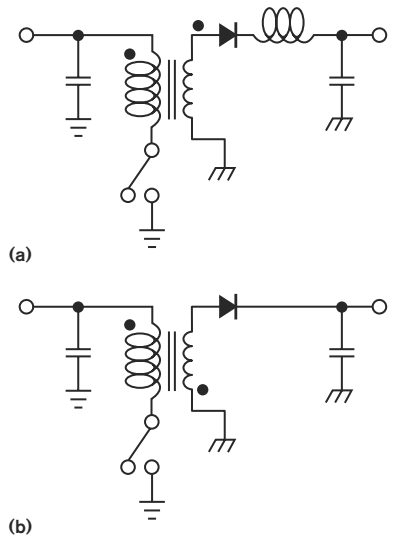



Figure 4 Common isolated converters include the forward (a) and the flyback devices (b).

Offline-supply problems include inrush currents and harmonic currents. Inrush current is the large flow of current necessary for charging up the input capacitors at the moment of closing the input switch. This current can stress the rectifier diodes and cause early capacitor failure. Approaches to correcting this problem include the use of NTC (negative-temperature-coefficient) devices in series with the inputs (**Reference 6**). These devices offer a high resistance when they are cold. As the input current runs into the capacitor, the devices heat up, and the resistance decreases. Drawbacks can be the 190°C operating temperature as well as sensitivity to ambient temperature.

The second problem with offline supplies is that the input capacitors draw in large spikes of current. These spikes top off at every line cycle. Using PFC, which is mandatory on supplies sold in Europe, can reduce these spikes. Remember to fuse the electrolytic capacitors. Failing UL (Underwriters Laboratories) fire testing just before production is as calamitous as failing FCC and CE EMI/RFI (electromagnetic-interference/radio-fre-

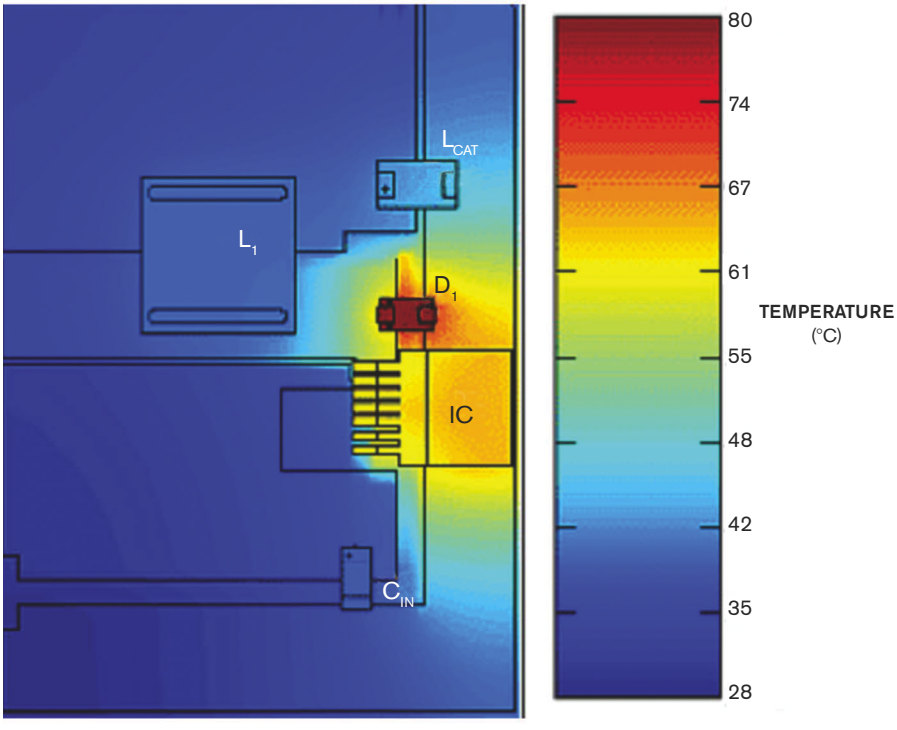
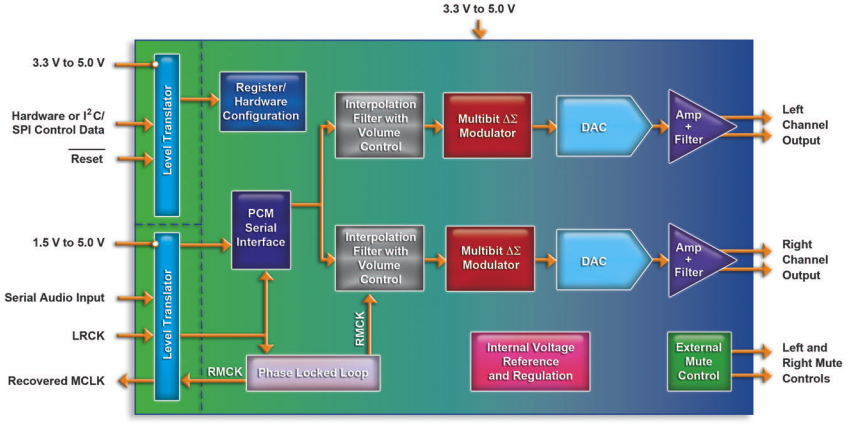


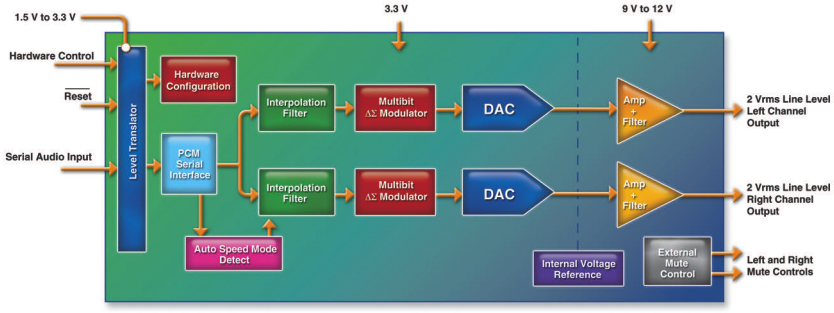

Figure 5 A thermal map shows that the freewheeling diode $D_1$ is the hottest component in the circuit (courtesy National Semiconductor).

# Stereo Digital-to-Analog Converters

## Integrated 2 $V_{RMS}$ Line Drivers and PLL Simplify Audio Designs




CS4350




CS4352

| Part | Dynamic Range | THD+N | Sample Rate | Analog Outputs | Power Supply | Comments | Package |
|---|---|---|---|---|---|---|---|
| CS4334/35/38/39 | 96 dB | –88 dB | 96 kHz | Single-ended | VA = 5 V | Entry-level Stereo DAC | 8 SOIC |
| CS4341 | 101 dB | –91 dB | 96 kHz | Single-ended | VA = 3.3 V or 5 V | Pin compatible with CS5341A, Digital volume control | 16 SOIC 16 TSSOP |
| CS4341A | 101 dB | –91 dB | 192 kHz | Single-ended | VA = 3.3 V or 5 V | Digital volume control | 16 SOIC 16 TSSOP |
| CS4344/45/46/48 | 105 dB | –90 dB | 192 kHz | Single-ended | VA = 3.3 V or 5 V | Upgrade for CS4340 and CS4340A | 10 TSSOP |
| CS4350 | 108 dB | –95 dB | 192 kHz | Single-ended or Differential | VA = 3.3 V or 5 V; VLC = 3.3 V to 5 V; VLS = 1.5 V to 5 V | Integrated PLL locks to incoming left-right clock | 24 TSSOP |
| CS4351 | 112 dB | –100 dB | 192 kHz | Single-ended | VA = 9 V or 12 V; VD = 3.3 V; VL = 1.8 V to 3 V | Line driver, 2 $V_{RMS}$ output | 20 TSSOP |
| CS4352 | 102 dB | –90 dB | 192 kHz | Single-ended | VA = 9 V or 12 V; VD = 3.3 V; VL = 1.5 V to 3.3 V | Line driver, 2 $V_{RMS}$ output | 20 TSSOP |
| CS4391A | 108 dB | –94 dB | 192 kHz | Differential | VA = 5 V; VL = 1.8 V to 5 V | DSD, pin compatible with CS4392 | 20 TSSOP |
| CS4392 | 114 dB | –100 dB | 192 kHz | Differential | VA = 5 V; VL = 1.8 V to 5 V | DSD, selectable digital filters, pin compatible with CS4391A | 20 TSSOP |
| CS4398 | 120 dB | –107 dB | 192 kHz | Differential | VA = 5 V; VD = 3.3 V or 5 V; VL = 1.8 V to 5 V | Flagship DAC, DSD processor, selectable D-filter | 28 TSSOP |

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- On-chip control and serial port level shifters
- Popguard® technology for control of clicks and pops
- Low-latency digital filtering

### CS4350 Features

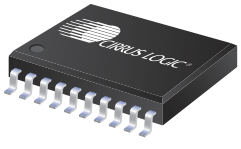
- Integrated PLL locks to incoming left-right clock—no MCLK required
- Supports PCM and TDM audio formats
- 108 dB dynamic range, –95 dB THD+N
- Single-ended or differential analog output architecture

### CS4352 Features

- Integrated line driver—2 $V_{RMS}$ output
- Compliant with consumer line level and SCART output
- 102 dB dynamic range, –90 dB THD+N
- Single-ended output architecture

### Applications

- Digital televisions
- DVD players and recorders
- Set-top boxes and DVRs
- Digital audio interfaces
- Effects processors
- Automotive audio systems





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quency-interference) testing.

Another common problem with off-line regulators using a switching IC is the quiescent current of the start-up circuit. You must provide 5 to 10V to the chip before any oscillation and regulation can begin. So, you must often use a large power resistor to feed this voltage to the chip. If you place the resistor across the 170V or higher dc bus to the 5 or 10V IC power rail, significant power dissipation will occur. Designers can in these cases use 500V Supertex depletion-mode FETs, but that option may be infeasible for low-cost supplies. Some vendors, such as Power Integrations, have developed alternative architectures to deal with this problem. "Solutions that use an integrated power transistor can derive the power for the control section by using the high-voltage MOSFET as a potential divider and tapping off a small amount of current at low voltage," says Doug Bailey, the company's vice president of marketing. "Power Integrations uses this approach in all of its switching ICs, and it works very well."

Digitally managed or controlled power uses a conventional analog PWM loop but hooks in substantial digital control, beyond the ubiquitous digital-shutdown pins on most controllers (**Figure 6**). Digitally managed power ICs first found use in battery-charger ICs. Older chemistries, such as lead-acid batteries, frequently used a voltage-regulator IC set to provide 2.3 to 2.36V per cell, depending on whether the application can tolerate higher charging voltages. Even these simple chargers often add ambient-temperature sensing, time limiters, or cell-temperature sensing to adjust the charge voltage. Nickel-metal-hydride and, to a greater extent, lithium-ion chemistries require even more digital supervision and manipulation. The system designer may want to terminate the charge cycle based on a rise in temperature or a rise in voltage. You should not start full-power charging if the battery is dead. If this situation occurs, the charger IC must "burp" a little current into and monitor the cells until the voltage becomes high enough to accept full-power charging. If the battery has been charging for several hours and still has not achieved termination, the IC should end the cycle. Ambient-temperature faults and many other variables may also be pertinent. "We no longer think of a battery-charger IC as a PWM circuit with some logic," says Mary Kao, an application engineer at National Semiconductor. "We look at it now as a microcontroller with an analog-PWM section."

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Did you catch Paul's popular cover story on circulating currents? Read it at www.edn.com/article/CA6372822.

Once battery-charger ICs paved the way, many other applications demanded a large portion of digital control over analog PWM loops. For example, Xilinx FPGAs require strict power sequencing and control. One vendor, Cradle, makes a multicore-DSP IC. Because it is a 0.13-micron CMOS part and uses DDR SDRAM, the power-system design was challenging. The requirements include 3.3V for I/O, 1.2V for the core, 2.5V for the DDR-SDRAM I/O, 1.25 sink source for the DDR-SDRAM-impedance voltage, a DRAM voltage reference, and 1.8V for another IC. Cradle engineers Tapeng Huang and Craig Calder worked with Mike Cheong at Intersil to redesign five separate power outputs using a single multichannel controller. They have two dc/dc controllers, two dedicated DDR outputs, and two uncommitted low-dropout regulators. In a more familiar area, most PC enthusiasts know that the supply voltage to the processor and memory is under digital control. Handheld devices may have complex control requirements to conserve battery power and extend runtimes.

Digital power uses a DSP rather than an analog PWM loop to do the math to keep the loop stable (**Figure 7**). This

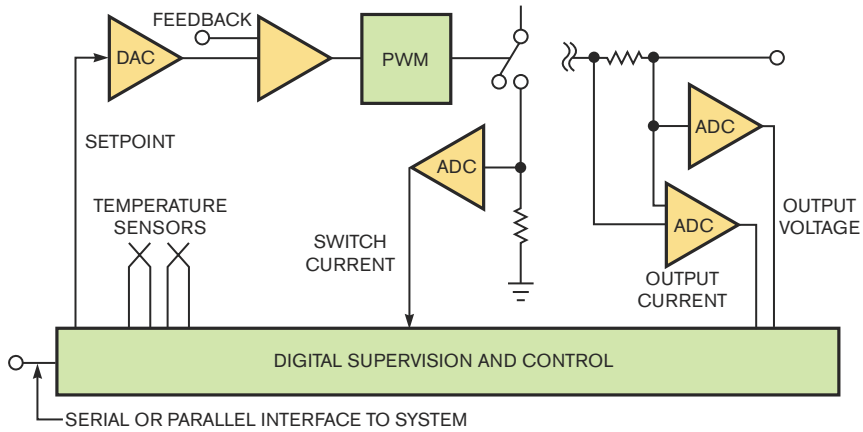


Figure 6 Digitally managed power uses a conventional analog-control loop but has extensive digital circuitry to perform monitoring and control functions.

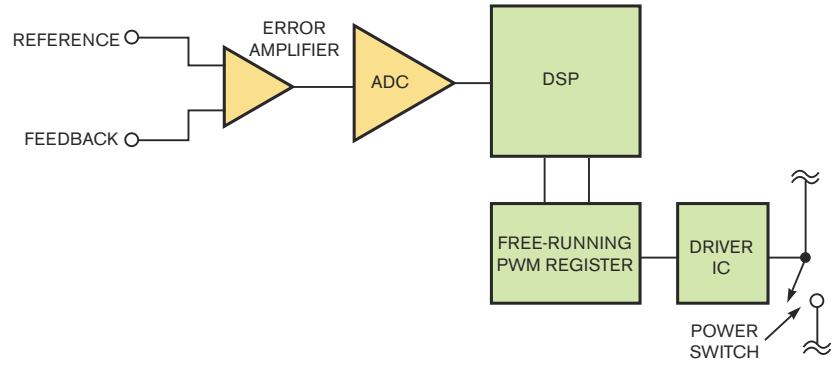


Figure 7 Digital power replaces the analog-control loop with a DSP or a digital-state machine.


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approach can provide flexibility in the loop compensation, but that flexibility comes at a price. Dave Mathis, a principal at Elandesigns points out: "If you are going to change the compensation, you have to be sensing something to base that change on. With acquisition times and error conditions, that is just asking for trouble." Indeed, experienced control-system engineers know that well-behaved systems usually have a single dominant pole. Nevertheless, Texas Instruments, Silicon Labs, and Primarion all make digital-power devices. Primarion has published articles stating that all power will be digital in the future and that analog engineers are only protecting their turf when they resist implementing digital power (**Reference 7**). Primarion does not use a DSP to manage the control loop. Rather, the company employs a free-running state machine that uses far less power than a DSP. Still the control is in a digital loop rather than an analog PWM loop. Steven Bakota, manager of digital power at Texas Instruments, points out: "Digital power is nothing new. TI has been selling digital power for 10 years … in the form of libraries to use with standard DSPs. The difference now is that we have our Fusion line of custom-built parts and a software-development environment to ease the implementation of the design."

Diligent power-supply designers must remember that 60,000 transistors in a DSP provide the control loop of a digital-power system, whereas an analog approach requires only about 100 transistors. Digital-power aficionados also brag about quiescent-power consumption of 7 mA. That figure may be acceptable in a blade server that operates from a wall outlet, but no battery-operated or portable product could afford that much power loss. An analog approach, in contrast, can operate at less than 1 mA. Designers should also evaluate a momentary power loss on the system. If the DSP has to reinitialize and run user-written code after a supply transient, that may make the supply unsuitable for some applications. A final caveat is that managers have to be willing to put a complex software-development effort right at the end of a product's design cycle, which is typically when the power subsystem is designed. Managers should not be lulled by promises of triviality in the design. If the design was trivial, an analog PWM part could do it at lower cost and less quiescent current. Make sure that a digitally managed system is not more appropriate than full DSP digital control of the loop. **EDN**

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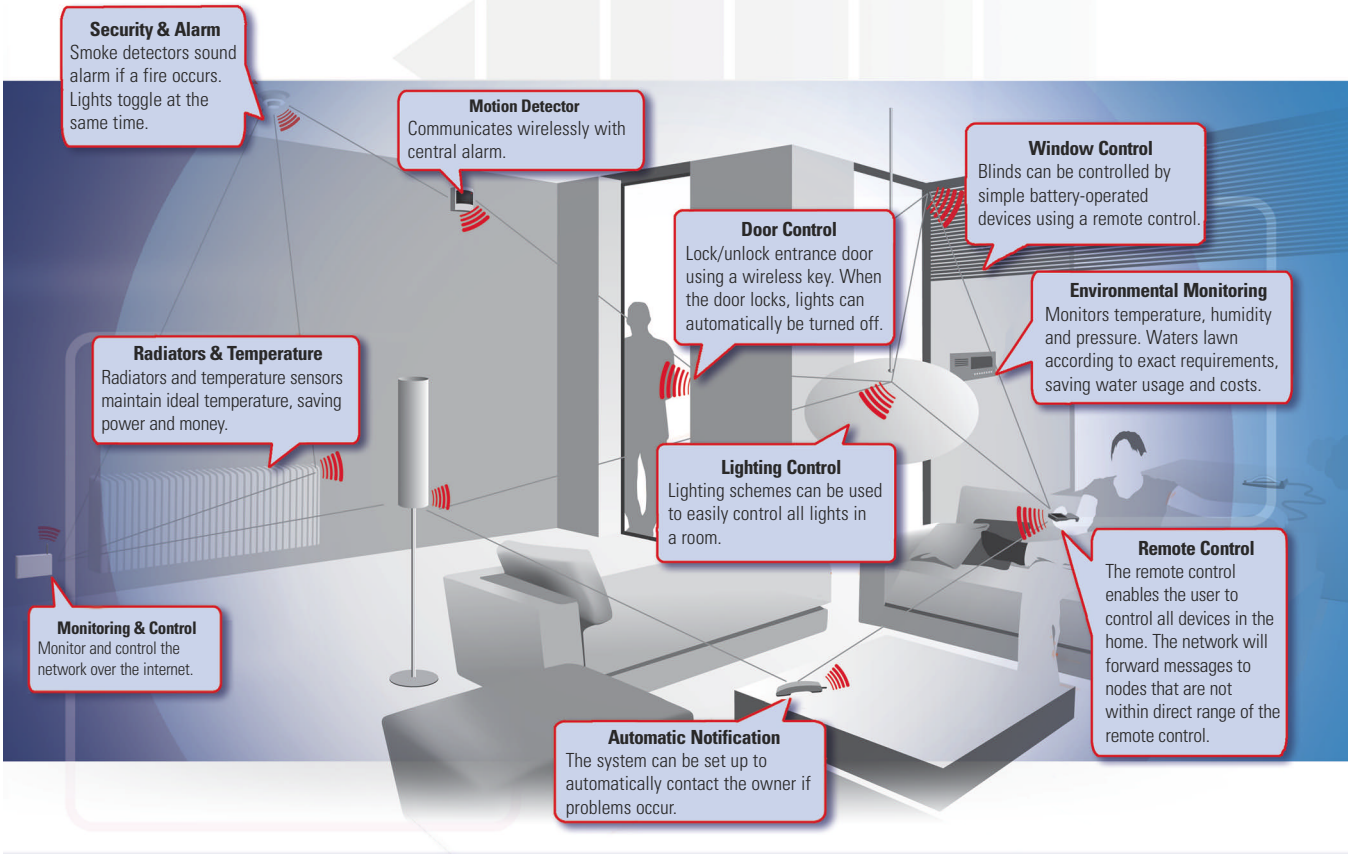
You can reach Technical Editor Paul Rako at 1-408-745-1994 and paul.rako@reedbusiness.com.

# ZigBee™ Wireless Communications Overview

3Q 2006




With a ZigBee wireless network, your home devices can easily be connected to each other. A wireless home automation system dramatically reduces installation cost and time, saves energy and makes it easy to add new devices.

**Chipcon Products from Texas Instruments**

## What is the ZigBee™ standard?

The ZigBee standard was developed for wireless communications. It was developed by the ZigBee Alliance, which is a global ecosystem of over 200 major OEMs creating wireless solutions for home, commercial and industrial applications.

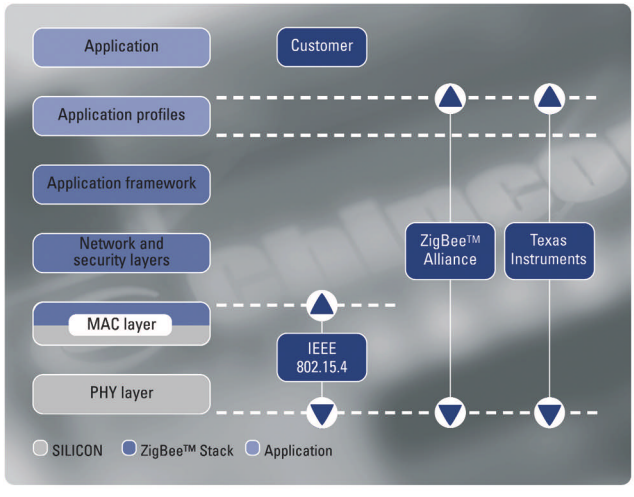
It is the only global wireless communications standard that allows the development of easily deployable, low-power monitoring and control products. The ZigBee Alliance is supported by several multi-billion dollar OEMs, as well as major suppliers.

### Primary target markets

- Building and industrial automation
- Home control/security
- Medical
- Logistics and asset tracking
- Sensor networks
- Active RFID

ZigBee technology is being embedded into a growing number of products across consumer, commercial, industrial and government markets worldwide. The ZigBee communication standard is key to the growth of wireless home and building automation applications where various end products need to communicate with each other.

This is enabling companies to have for the first time a simple, reliable, low-cost and low-power standard-based wireless platform optimized for the unique needs of remote monitoring and control applications.




ZigBee Platform

## Why the ZigBee standard?

The ZigBee standard is the only standard that specifically addresses the typical requirements for wireless control and monitoring applications such as:

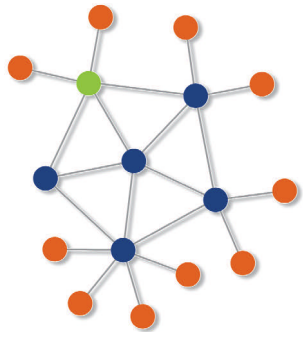
- Large number of nodes/sensors
- Very low system/node costs
- Operation for years on inexpensive batteries
- Reliable and secure links between network nodes
- Easy deployment and configuration
- Global solutions

For OEMs, it is much more cost effective to design applications based on the standardized ZigBee technology than create a new proprietary solution from scratch. Furthermore, OEMs can obtain global solutions and independence from RF IC vendors due to the 2.4GHz standardized radio by IEEE 802.15.4. Existing manufacturers of wired field bus technologies who migrate to the ZigBee standard will not only reduce installation costs for their customers, but will also reduce their product's bill of materials due to the cost-effectiveness of ZigBee-compliant solutions.

## ZigBee-compliant platform

Texas Instruments (TI) offers customers a complete hardware and software ZigBee-compliant platform that has been certified by the ZigBee Alliance. The platform is a reference design, which includes the IEEE 802.15.4 PHY/MAC and the ZigBee stack up to and including the application framework. This forms a solid base for ZigBee system development. In addition, TI supports all application profiles approved by the ZigBee Alliance. Customers who base their development on TI's certified ZigBee-compliant platform will shorten time to market and reduce costs for their system design and ZigBee end-product certification. Furthermore, customers who use a public ZigBee Application Profile are ensured full interoperability with other ZigBee systems that use the same profile.

ZigBee™ Alliance
Wireless Control That Simply Works



**PAN Coordinator**
(Full-Function Device)

**Coordinator**
(Full-Function Device)

**Device**
(Reduced or Full-Function)

## ZigBee mesh networking

Above the PHY and MAC layers defined by IEEE 802.15.4, ZigBee specifications enable reliable and secure mesh, star and cluster-tree network topologies with interoperable application profiles. Mesh networks allow for high levels of reliability and scalability by providing alternative routes through the network.

### TI ZigBee goals:

- To provide consumers with ultimate flexibility, mobility, and ease of use by building wireless intelligence and capabilities into everyday devices.
- Enable customers to have a simple, reliable, low-cost and low-power global standard-based wireless platform optimized for the unique needs of remote monitoring and control applications.

## TI low-power RF products for ZigBee

| Product | IEEE 802.15.4 ZigBee-compliant Dev. Platform | Transceiver | System-on-Chip |
|---|---|---|---|
| CC2420 | X | X | |
| CC2430 | X | | X |
| CC2431* | X | | X |

* With integrated location engine

- IEEE 802.15.4/ZigBee-compliant development kits
- High-performance radio and robust reference designs
- Free IEEE 802.15.4 MAC software

### ZigBee TI software development suite:

- Z-Stack™: Industry-leading ZigBee-compliant protocol stack
- Z-Stack protocol stack extensions
- Z-Trace™ (debug tool)
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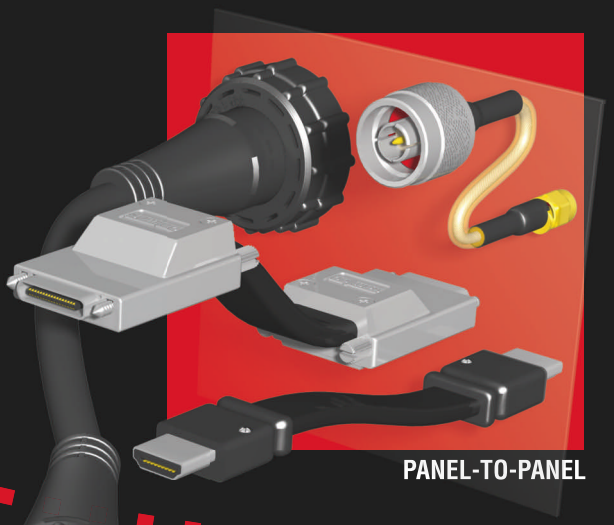

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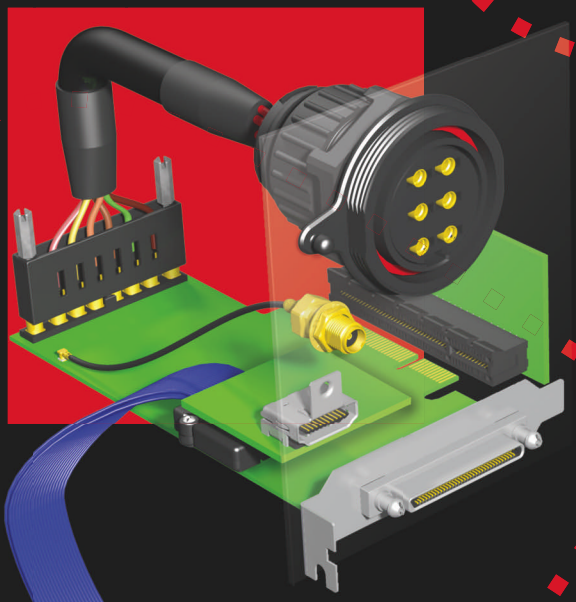

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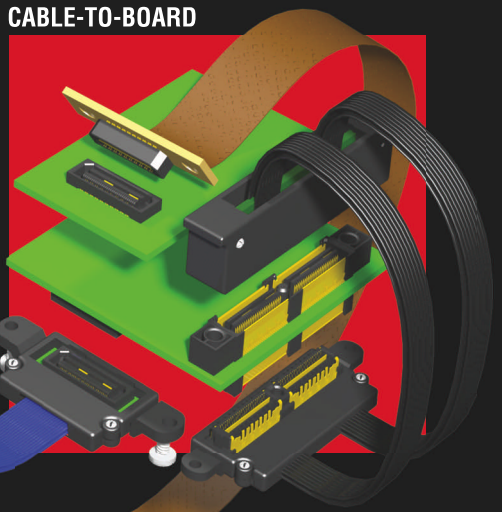

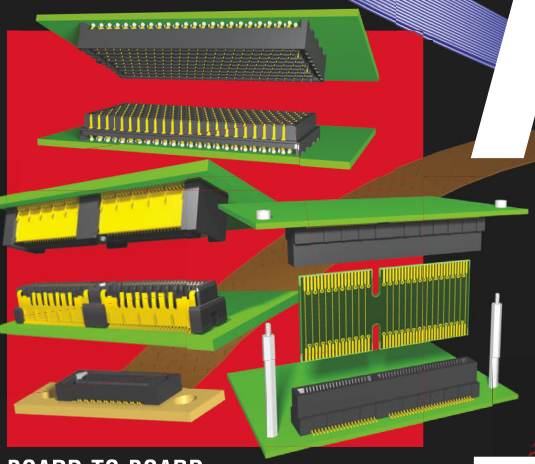

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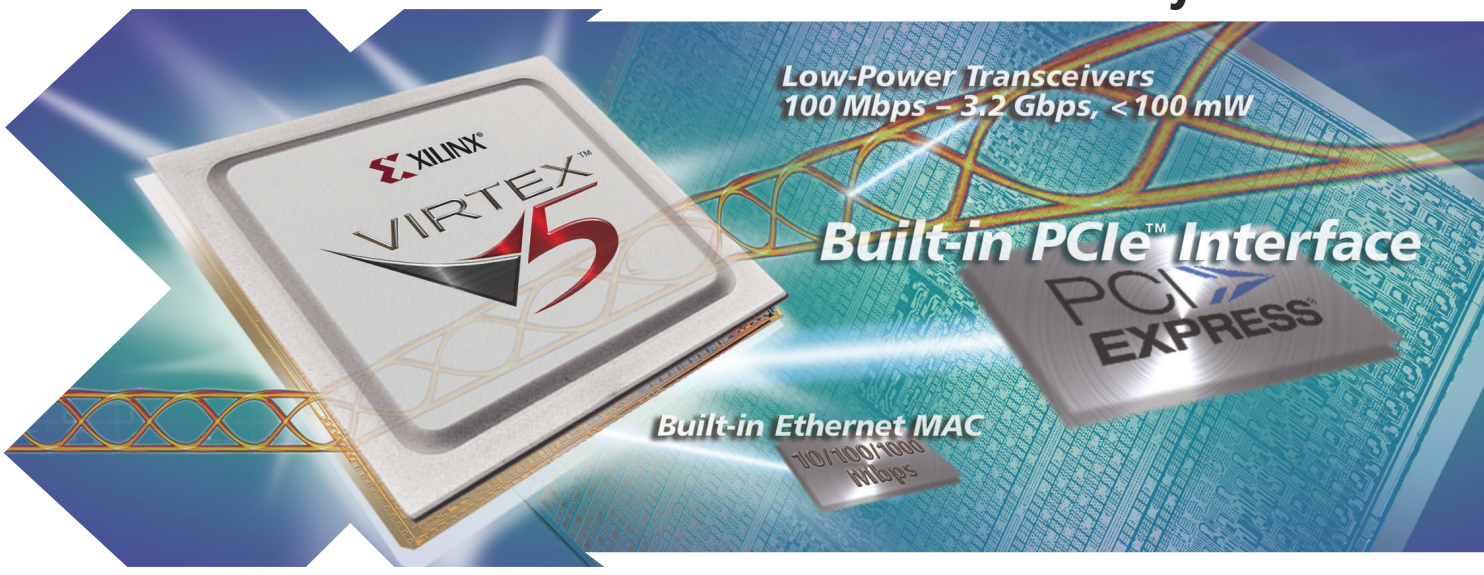


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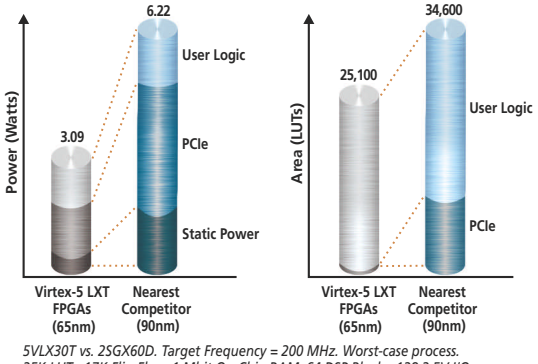


*5VLX30T vs. 2SGX60D. Target Frequency = 200 MHz. Worst-case process. 25K LUTs, 17K Flip-Flops,1 Mbit On-Chip RAM, 64 DSP Blocks, 128 2.5V I/Os. Based on Xilinx tool v8.2 and competitor tool v6.0.1*

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# Battling bugs

DEBUGGING EMBEDDED SYSTEMS CAN REPRESENT MORE THAN HALF OF AN EMBEDDED-SOFTWARE-PROJECT WORKLOAD. UNDERSTANDING HARDWARE-DEBUGGING FUNCTIONS AND THE ISSUES THEY TACKLE IS KEY TO SELECTING THE RIGHT CHIPS, BUILDING DEBUGGING SYSTEMS, AND INCREASING PRODUCTIVITY.

Many people erroneously credit the term "bug" to Rear Admiral Grace Murray Hopper. In fact, however, no one knows where the term originated, and it may go back to Thomas A Edison or even earlier. Nevertheless, US Naval Reservist Hopper found a moth that had short-circuited Relay #70, Panel F, of the Mark II Aiken Relay Calculator while it was being tested at Harvard University on Sept 9, 1945. By removing the moth—that is, "debugging" the computer, she solved the glitch that had temporarily shut down the machine (**Reference 1**). Although that early example literally removed a bug from a system's hardware, "debugging" today refers to the process of understanding a program failure and removing the defective code. A failure includes any small deviation from the original intention, and removing the defective code is much better than adding correction code. In an ideal situation, all characteristics, such as bus and register values of a system, would be accessible at any time for monitoring and modification. But with ICs moving toward SOCs (systems on chips), accessibility becomes more difficult.

Debugging hardware is about providing as much access as possible to the internal resources of an embedded system, either through observing characteristics of the system, such as CPU states and PC values, or by changing system parameters. You can debug embedded systems in the early stages of design with simple techniques, such as logging and monitors, or you can use more recently developed methods for multicore SOCs, such as tracing, cache debugging, and cross-triggering. This article focuses not on how to write or debug the code, but on which embedded hardware IP (intellectual property) is available and which aspects of debugging this IP addresses.

## LOGGING AND MONITORS

The oldest and most common method of debugging is to add print statements in the code to show information about which pieces of the software execute and provide insight into the actual values of registers and variables. This exercise may be a legacy of the first-year-student exercise "hello world," in which the appearance of the two words on the screen prove that the program was alive and has executed up to a certain point. The print statement, or printf, is just one variant of logging, the process of using the processor to write important information to a "pipe" for external tracing. The pipe you use depends on the system; in the printf case, the pipe is the standard output (screen), but it can also be a UART, a USB, or even general-purpose I/O.

Logging can be valuable when you need to structure component information in a way that is meaningful to the programmer, such as providing sensor information or state-machine transitions. You can use logging tools to analyze logging information and generate a postprocessing database. To achieve efficiency, you must carefully employ logging functions. For example, logging messages should start with keywords, such as "warning," "error," or "debug" and should identify the message initiator. You should group logging functions in a small set of files for easier maintenance and provide time-stamp information if available. Unfortunately, logging is intrusive and modifies the software's real-time behavior to be unlike that of the final application.

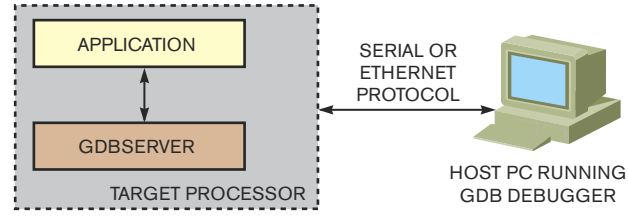


Figure 1 Gdbserver for the Linux operating system is an example of a debugging monitor that runs on the target while communicating with a host debugger.

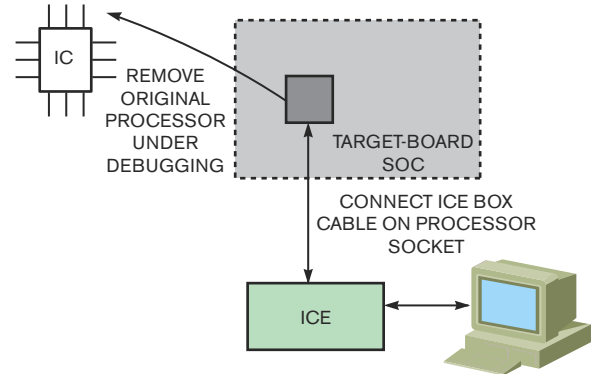


Figure 2 In-circuit emulators feature modified processor hardware where internal buses and state signals are bonded out and made available to the user.

The debug monitor, another popular debugging tool, works with code running on the target (**references 2** and **3**) in the CPU memory. A debugger running on a host communicates with the monitor through a dedicated port to send commands and receive responses. You can consider the gdbserver program for Linux, although more complex than early ROM monitors, as a debugging monitor (**Figure 1**). When a user wants to set a breakpoint on an instruction, gdbserver saves the instruction and replaces it with a system call. Gdbserver then relies on the ptrace program from Linux to get information on all applications doing system calls. Subsequently, the gdbserver can take control of the application you are debugging when the system call occurs to invoke the breakpoint. The debugger runs on a host machine and connects to the target through a serial or Ethernet connection (**Reference 4**). Monitors are cheap and practical but have several disadvantages, such as the need to load the code before any debugging and possible interaction with application software. You cannot use monitor software if code resides in flash because it needs to patch the application to insert software breakpoints.

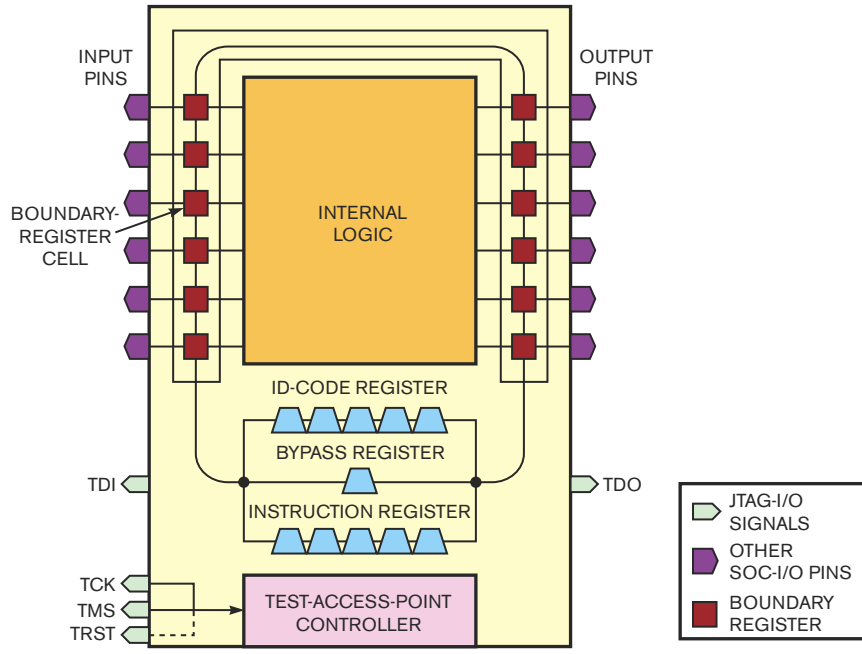


Figure 3 The IEEE 1149.1 JTAG standard defines a limited I/O port with as many as five signals to perform testing and analysis of circuits through serial communication.

## IN-CIRCUIT EMULATION

The first hardware-based debugging technology, the ICE (in-circuit emulator), is a version of the processor you are debugging. ICEs usually employ an FPGA (field-programmable gate array). FPGAs bond out their internal buses and state signals and make them available to the user (**Figure 2**). ICEs provide more debugging capabilities than do ROM monitors. To use ICEs, you must replace the processor you are debugging on a board by a connection to an ICE box. A host running and emulating the functions of the debugger controls this box. One of the primary limitations of the ICE is its high cost. Additionally, although the method suits simple processors, modern SOCs with increasing complexity, integration, and frequencies make it difficult for IC vendors to provide ICE versions for the modern processors.

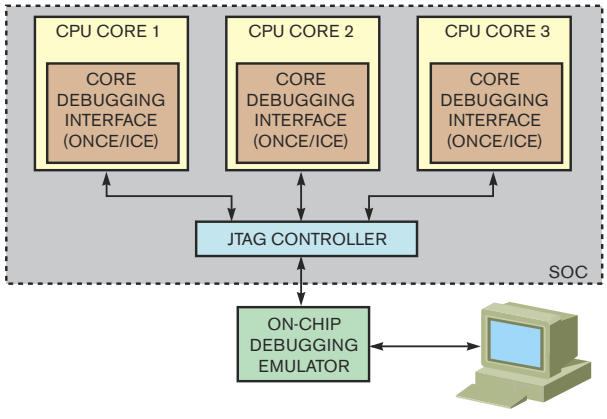


Figure 4 In the case of multiple processors on a single chip, debugging hardware communicates directly with the main JTAG controller.

In 1985, a group of European companies formed the JTAG (Joint Test Action Group), a consortium to overcome the problems of testing semiconductor ICs. They created the IEEE 1149.1 standard for boundary-scan testing of ICs, which they released in 1990 (**Reference 5** and **Figure 3**). The JTAG standard defines a limited I/O JTAG port with as many as five signals to perform testing and analysis of circuits through serial communication: TCK (test clock), TMS (test-mode select), optional TRST (test reset), TDI (test-data in), and TDO (test-data out).

The IEEE based JTAG hardware on a 16-state finite-state machine, which the TMS signal controls. The TCK's rising-edge clock captures this TMS signal. The data information shifts in on the TDI pad and shifts out on the TDO pad. You eventually use TRST to reset the design. You add scan registers for each pad of the IC and connect them internally to form a boundary-scan chain. You can shift this chain in and out through TDI/TDO and JTAG commands to test the external connections on a board, test the logic connections inside the IC, capture values of the pads, and put the JTAG chain in bypass mode. JTAG provides low-cost

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manufacturing-test capabilities, and it has become the most common method for testing. But, due to its ease of use, high availability, and low-cost implementation, designers also frequently use JTAG as a debugging port to access on-chip debugging resources (**Reference 6**). JTAG is the transport layer of debugging communication between a debugger running on a host and the embedded processor's debugging resources. Instructions shift into the instruction register to access the debugging hardware IP. Due to the increasing cost of ICEs, many semiconductor vendors integrate more debugging hardware on-chip to cope with debugging limitations and provide similar functions to the ICE. One popular implementation of such on-chip debugging hardware is the BDM (background debugger mode) from Freescale Semiconductor Inc (www.freescale.com, formerly, Motorola) on 68-kbit Coldfire embedded processors and PowerPC (now, Power Architecture) processors. Other vendors use proprietary names for similar functions.

On-chip debugging hardware adds some functions, such as hardware breakpoints, internal register access, read/write to memory, and watchpoints, which you could previously access only through an ICE. In a multiprocessor SOC, you can connect each piece of chip-debugging hardware to the main JTAG controller. The connection may vary depending on the vendor, but the typical implementation creates a TDI-TDO JTAG chain between the on-chip debug JTAG state machines and the host debugger (**Figure 4**).

## TRACING

One of the biggest issues in real-time-system debugging is the Heisenberg bug, or probe effect: Any software or hardware you add for debugging or monitoring is likely to change the real-time system's behavior. This situation can happen when you add software to collect information for profiling, debugging, or monitoring. You can see a similar impact when using debugging hardware. For example, on-chip debugging hardware may modify the processor execution flow to insert breakpoints or profiling hardware may "steal" part of the processor bandwidth to memory to store profiling information.

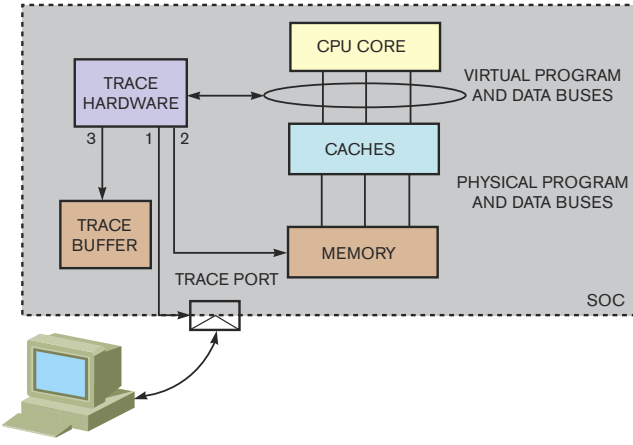


Figure 5 An on-chip trace-hardware architecture minimizes debugging interaction with separate buses for trace data and processor data.

Debugging hardware may also use the UART connection to log information when the production software is supposedly using this interface. ICE usually provides nonintrusive trace capabilities in which the developer can access the program counter of the processor at any time. More SOC vendors are integrating trace hardware on-chip to provide similar functions (**Figure 5**). Trace hardware achieves nonintrusiveness through the use of dedicated trace hardware, a dedicated trace port, separate data buses for trace data and processor data, and a JTAG interface.

You can capture trace information using a trace port. In this method, you connect a trace box or a logic analyzer on the trace port to reconstruct the messages and correlate them with source code. Another method of capturing trace information is to use a virtual trace buffer, in which the processor's memory stores trace information and the host retrieves it—through the JTAG port, for instance—once the test ends. A third alternative is to use a dedicated trace buffer in which a dedicated memory stores the trace information, which the host retrieves once the test ends.

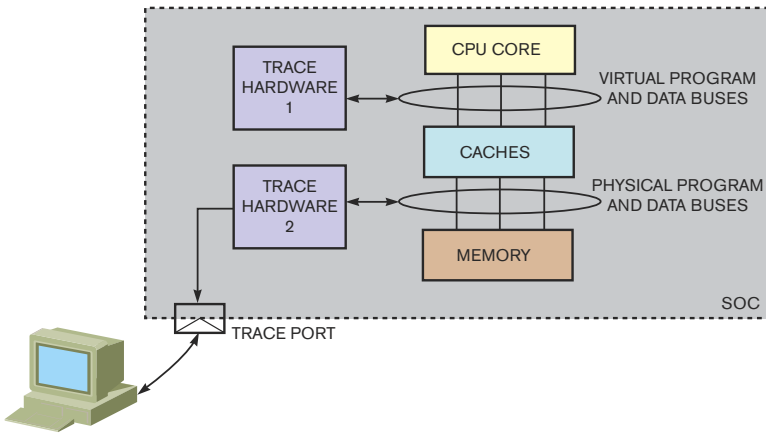


Figure 6 Embedded hardware allows the user to trace buses before and after on-chip caches to better understand the cache behavior.

The IEEE-ISTO 5001TM 2003 Nexus 5001TM Forum Standard for a Global Embedded Processor Debug Interface provides an open, general-purpose interface for the software development and debugging of embedded processors (**Reference 7**). The Nexus Forum started its work in 1998 and issued its first release of the Nexus standard in 1999 with updates in 2003. The goal was to build on several vendors' experience in embedded-system debugging and tools to standardize on-chip-debugging features and interfaces. Because several of the vendors in the forum already offered proprietary products for on-chip debugging, the requirements for basic on-chip debugging are general enough to ease Nexus compliance. The benefit is the standardization of the Nexus trace interface, such as trace features, signals,

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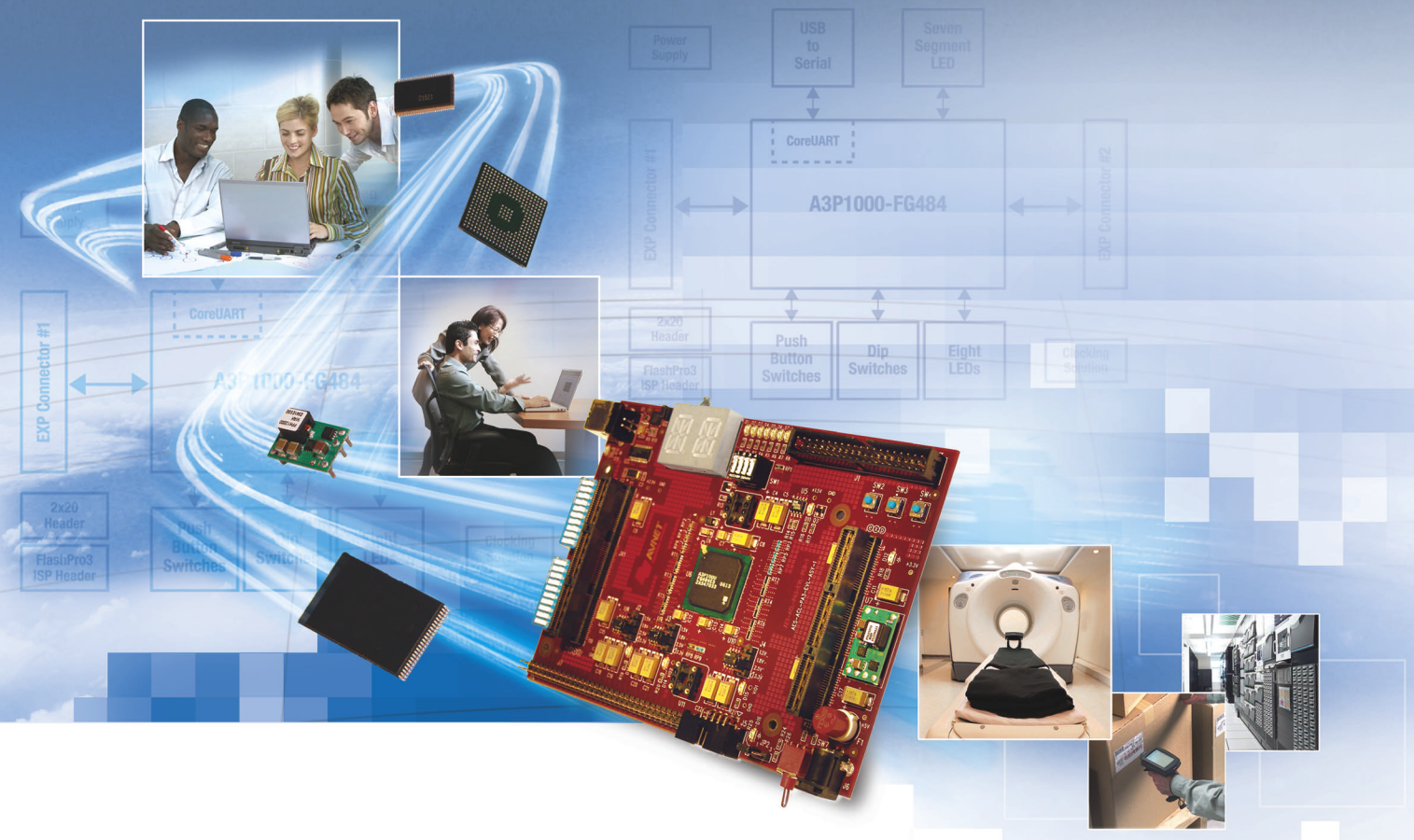


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messaging protocol, and APIs (application-programming interfaces). Meanwhile, standardization leaves enough room for vendor-defined customizations. Initially targeting automotive applications, the Nexus standard has rapidly spread in the wireless and networking markets.

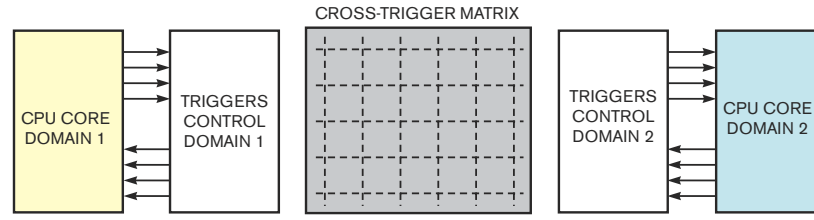


Figure 7 Users can create complex debugging sequences with cross-triggering, which translates events from one core domain to generate triggers in another core.

## MULTICORE DEBUG

Caches provide high performance but are difficult to debug because they hide the CPU's execution from the external memory buses, and the coherency between cores and DMA or acceleration hardware is hard to understand. Embedded trace hardware is helping to solve this problem because the bus under trace is usually virtual (before the caches), not physical. It may also be very helpful to trace buses before and after caches to better understand the cache behavior (**Figure 6**). Comparison of the resulting two traces provides good indication of the cache misses, when the cache generates accesses on the physical bus. This approach helps to reduce cache misses and enhance the performance of the software. Another option is to add embedded cache-debugging hardware to read the cache content in debugging mode or write into cache. This option is usually in the form of cache-debugging registers accessible through software or JTAG ports. With a debugger, a user can halt the program execution and check the cache's content. The user can employ this information to debug cache-cleaning issues, such as invalidation, synchronization, or flushing.

Modern SOCs often integrate several processors on one chip, and it becomes difficult to debug the interaction of the cores with traditional debugging hardware. Cross-triggering, a recently emerging debugging technique, has become popular for debugging complex multicore SOCs (**Reference 8**). The principle is to translate events from one core domain to generate triggers in another core's domain or to the same core domain. Typical events are entry into debugging mode, interrupt occurrence, watchpoint occurrence, and breakpoint occurrence. Input triggers are typically debugging requests. Triggers generate a debug request, an interrupt, or a glitch

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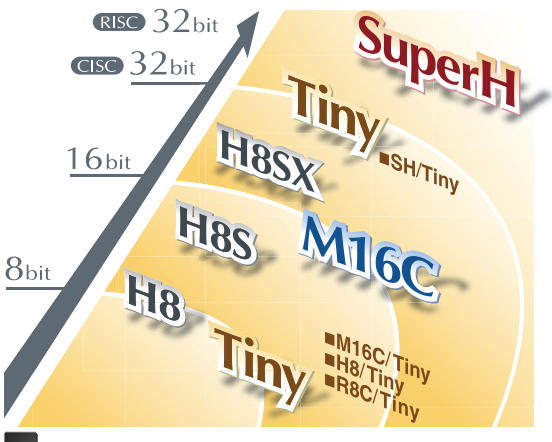


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on one SOC pad. They can also start or stop the trace on the processor. The combination of triggers leaves all flexibility to the end user to create complex debugging sequences. You can use cross-triggers to start a trace on Core A when Core B reaches a specific program address or to stop Core B's activity when Core A enters debugging, for instance.

With increasing pressure on SOC sizes, low-cost debugging may be the Holy Grail for embedded-system architects. But they must keep one thing in mind as their priority: Never compromise the debug capabilities of the system. If they couldn't anticipate all the bugs of their systems, they should at least increase their chances of capturing them in the future. The cost savings of reduced embedded debugging hardware may be at the expense of higher software-debugging costs later in the project. They should also remember that debugging and security have contradictory requirements. Many manufacturers now ship products and simply disable the debugging features to protect themselves from hackers. This practice is unwise. You can never anticipate the type of issues you will encounter in the field. Protecting debugging access with security methods, such as keys or fuses, is a better option that will not jeopardize your debugging capabilities. **EDN**

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## AUTHOR'S BIOGRAPHY

*Bertrand Déléris is a systems-architect engineer at Freescale Semiconductor Inc (Toulouse, France), where he has worked for seven years. He graduated from the engineering school of the National Institute of Applied Sciences (Toulouse, France) and has a master's degree in research from the Paul Sabatier University (Toulouse, France). His personal interests include playing the guitar and reading books.*

# DAQ Attack

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**2** The name of the high-performance, multithreaded, NI data acquisition driver
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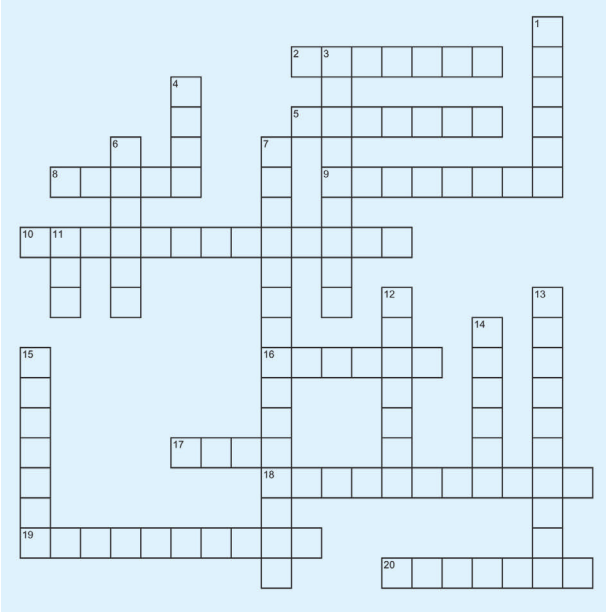
**8** Unwanted signals
**9** A measure of the capability of a DAQ system to faithfully indicate the value of the measured signal
**10** Containing one or more type of I/O operation on a single device
**16** Annual conference of virtual instrumentation held in Austin, TX
**17** A semiconductor device containing programmable logic components that can be reprogrammed based on varying functionality requirements
**18** Devices that convert a physical phenomenon into a measurable electrical signal
**19** 18 bits of this provides 262,144 discrete levels
**20** He helped discover that a signal must be sampled at least twice as fast as the bandwidth of the signal to accurately reconstruct a signal



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**6** Butterworth, Chebyshev, Elliptic, Bessel, etc.
**7** Acquiring two or more different signals at the same time
**11** PC-bus with external connection for hot-swappable, plug-and-play operation
**12** Industry leading data acquisition series of devices from NI
**13** New high-speed PC-bus with serial, point-to-point topology
**14** Fundamental components used to digitize and generate analog signals
**15** An event that occurs in order to begin an acquisition or generation

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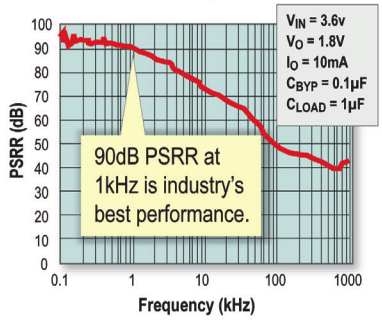
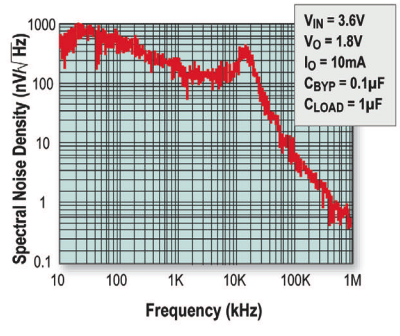



**ISL9000 SPECTRAL NOISE DENSITY vs FREQUENCY**

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| | PSRR at 1kHz | Output Noise Vrms @ 100µA (1.5V) | $I_{OUT}1$ (max) mA | $I_{OUT}2$ (max) mA | $I_Q$ (typ) µA | Voltage Accuracy |
|---|---|---|---|---|---|---|
| **ISL9000** | 90dB | 30µ | 300 | 300 | 42 | 1.8% |
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| **ISL9011** | 70dB | 30µ | 150 | 300 | 45 | 1.8% |
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# Embedded memory evolves

## IN THE SEARCH FOR ON-CHIP RAM, SOI TECHNOLOGY OFFERS A NEW ANSWER.

Ever since its invention in the 1970s, DRAM (dynamic RAM) has been the most popular form of semiconductor memory. Indeed, modern computing and communication systems could not exist without DRAM. The first volume-production device had a capacity of only 4 kbits, but, within 30 years, the capacity has increased a millionfold. At about the same time that DRAM emerged, the microprocessor appeared, evolving from early calculator chips. This development quickly led to the development of the PC. When people started trying to use these new marvels, two limitations became apparent: The processor chip needed to be faster, and more memory was necessary. The same pressure for processor speed and memory size came from the communications sector, with the result that logic and memory have followed two divergent evolutionary paths.

### LOGIC AND MEMORY DIVERGE

The drive for speed in processors led to the development of logic processes to produce transistors with fast-switching characteristics. Power consumption and, to some extent, cost were not primary considerations. Process scaling enabled vast numbers of transistors to find use in designs, and the lower voltages these designs employed mitigated the rise in power consumption. But, with fast transistor switching came leakage, which, together with low-voltage operation, made the inclusion of DRAM in ASICs effectively impractical. In recent years, the upward trend in switching speed has reached a saturation point, and processor designers have employed architectural developments such as multiprocessor configurations to achieve greater performance. However, one recent technological development—the move from bulk silicon to SOI (silicon-on-insulator) structures—has provided a step-function increase in processor performance. Following this trend, AMD (Advanced Micro Devices, www.amd.com) has announced the move to SOI for its new processor families (**Reference 1**).

While processors were chasing speed, DRAM continued to emphasize size. Every couple of years, manufacturers were introducing a new process reduction. They developed the trench and stacked capacitors to cram more memory cells into a unit area. But the manufacturers emphasized size and cost, rather than performance. So, memory processes became more complex for each generation, diverging from logic processes. As time passed, memory and logic processes became more and more incompatible.

Fast-forward to the 1990s with the introduction of digital phones, digital TV, and the Internet, spawning a massive demand for sophisticated personal electronics. The use of complex ASICs, almost always containing a processor and memory, made these products economically viable. The high-performance processor communicated with on-chip SRAM (static RAM) because SRAM macros were both fast and compatible with logic processes.

Now, you need to know a little more history. Because DRAM development had gone down the large and cheap but slow path, DRAM couldn't match the speed demands of processors. Hence, the concept of cache memory evolved. Small and fast, cache memory stores a segment of the information that the bulk DRAM contains, with clever logic determining which data the processor is most likely to require next. Cache copies the selected "snapshot" of data from bulk memory before the processor makes the next memory access.

So, designers of cache memories employed the "forget-expense; make-it-as-fast-as-possible" principle. Technology limitations at the time meant that cache memories were not only expensive, but also small—just a few kilobytes. It was impossible to make small DRAMs because of the overhead

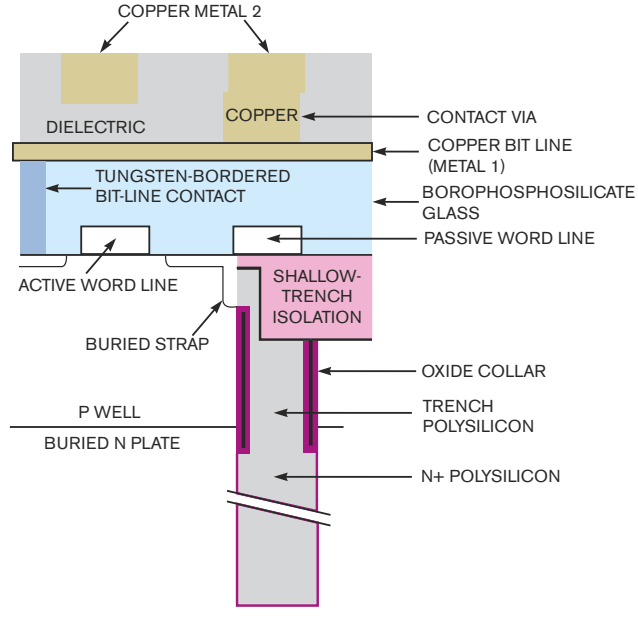


Figure 1 IBM's embedded DRAM stores charge on the walls of a deep-trench structure.

of the refresh logic necessary to restore the data that would otherwise fade away after a few milliseconds. Therefore, manufacturers made cache memories using SRAMs, which required no refresh. The application in cache memories pushed SRAM development along the same evolutionary path as microprocessors. They had to be fast, so they thrived on the same logic-process improvements as microprocessors; this co-evolution meant that they remained process-compatible.

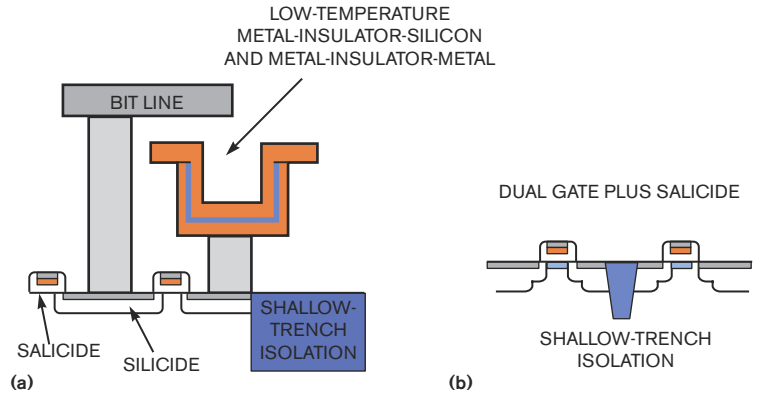


Figure 2 NEC's stacked-capacitor embedded DRAM (a) uses a metal-insulator-metal capacitor above the silicon in the interconnect stack (b).

## JOINING DRAM AND LOGIC

In the 1990s, designers were building ASICs using embedded processor cores and embedded SRAM. They used SRAM because they had always done so and because they believed that DRAM was much slower and incompatible with ASIC processes. However, researchers at IBM (www.ibm.com) suspected that these beliefs were not necessarily true. They postulated that designers could build DRAM to be almost as fast as SRAM and to occupy less chip area (**Reference 2**).

In parallel, researchers at the IMEC (Interuniversity MicroElectronics Center, www.imec.be) in Leuven, Belgium, were studying a parasitic phenomenon that occurred with SOI devices. Because manufacturers fabricated the MOS transistors in electrically isolated islands, they could accumulate charge. This charge, or "floating-body" effect, influenced the current that would flow when you apply voltage to the gate. The researchers concluded that they could harness this effect to make a memory device—DRAM—and filed a patent. They encountered problems, however. The effect was difficult to control, and, when they fabricated a memory array, activity in one cell tended to cause adjacent cells to switch. The technical hurdles at the time were too formidable, and the researchers let the patent lapse.

Now, fast-forward to 2000 and beyond. IBM had figured out how to make fast DRAM and make it compatible with logic processing. The company started to offer embedded DRAM as part of its ASIC portfolio. NEC (www.necel.com) has taken the same tack. Meanwhile, Serguei Okhonin, PhD, and Pierre C Fazan, PhD, had cracked the problems of making floating-body-effect DRAM work. The two men formed a company, ISI (Innovative Silicon Inc, www.innovative silicon.com), to develop and exploit the invention, which they patented as Z-RAM (zero-capacitor RAM). In early 2006, AMD licensed the ISI floating-body-effect-memory IP (intellectual property).

Now, two approaches are available for building high-performance processors and ASICs: Either build in bulk silicon CMOS with compatible embedded DRAM, or build in SOI using the floating-body-effect DRAM. Many engineers' immediate reaction to this choice is to point out that SOI wafers are 10 to 15% more expensive than bulk silicon, making any use of SOI appear more expensive. However, several facts about SOI design make this observation incorrect in practice.

First, because of the nature of SOI circuits, a given design can occupy less die area and operate as much as 35% faster than an equivalent design in bulk CMOS. Second, die yield falls by approximately one-fourth the power of the die size, so any die-size reduction immediately translates to a major saving in cost. Clearly, these two factors work together on cost for good dice. ISI estimates that, if embedded memory occupies more than 18% of the die area, the smaller die resulting from using Z-RAM generates a cost saving that counterbalances the extra cost of SOI wafers and processing. The bigger the memory, the greater the cost advantage—along with the speed and power improvements of SOI.

And the comparison to bulk CMOS is itself not quite accurate. Although manufacturers can make embedded DRAM process-compatible with logic, the DRAM still requires a trench or stacked capacitor to provide sufficient charge storage for reliable operation. Fabricating this capacitor requires additional process steps, some of which are critical. But floating-body-effect DRAM on SOI requires no additional capacitor and no additional process steps. All this approach requires is standard logic processing.

## KEY MEMORY PARAMETERS

Memory has become the largest single component in modern high-performance processor-chip designs. Hence, choosing the optimum design compatible with high-performance logic is critical to a new design's success. Designers must consider many parameters, including cell size, standby power, SER (soft-error rate), and performance.

**Cell size:** Dynamic cells tend to be five to seven times smaller than six-transistor static cells. However, using DRAM entails the overhead of voltage-level shifters and refresh circuitry. This overhead causes the area of dynamic circuitry to be only three to four times smaller than that of six-transistor cells.

**Standby power:** With SRAMs, background leakage current was once negligible. Unfortunately, with each process generation, the "device-off" or subthreshold leakage doubled to the extent that designers now must contend with static-memory cells that exhibit approximately 1000 times more leakage current on a cell-per-cell basis than dynamic cells. However, dynamic cells require level shifters and consume a refresh current. When you take these factors into account, embedded DRAMs tend to have a six- to eight-times power advantage over embedded SRAM.

**SER:** An SRAM would once hold its data without error

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indefinitely as long as the system maintained power. This situation is no longer always the case. A soft error occurs when a single bit flips to the opposite state, resulting in data corruption. High-energy particles, such as cosmic rays, which are constantly in the background in our environment, cause these errors. The susceptibility of a memory to soft errors is a function of the stored charge maintaining a given logic state in each cell. With embedded DRAMs in submicron technology, each cell holds approximately 20 times more charge per bit than SRAMs. Hence, embedded DRAMs tend to have as much as 1000 times fewer SER-induced failures than those in SRAMs, according to NEC (**Reference 3**). With SOI technology, no conduction can occur through the substrate; hence, embedded DRAM on SOI exhibits significantly better SER performance than bulk CMOS DRAM. You can mitigate the SER problem by including error-correction circuits within the memory array. However, these circuits cost silicon area, and the occurrence of multiple simultaneous "hits" can overwhelm them.

**Performance:** DRAM is not inherently slower than SRAM, but DRAM is unavailable during the refreshed cycle. So, when constructing a small memory with a simple interface, it would be natural to use SRAM. Several vendors now offer DRAM IP with built-in refresh and SRAM interfaces, so, for ASIC designers, it is no more difficult to use a DRAM block than an SRAM of the same size. When choosing between SRAM and DRAM, you must consider many density and performance trade-offs; however, the most important parameter is latency. "Latency" refers to the time interval between presenting a memory macro with a random data access and when that information becomes available. For a large ASIC containing a multiple megabyte RAM, the dominant element in latency is not the time to read the cells, but the time for the data request and its response to travel through the interconnect. Using a smaller die reduces this latency. In this case, embedded DRAM wins because, for a given memory size, DRAMS are three to four times smaller than SRAM. As an example, substituting DRAM for a 9-Mbyte embedded SRAM results in an area reduction of about 70% and a worst-case latency—that is, the longest signal path—reduction of more than 30% (**Reference 4**).

The field of bulk-CMOS embedded DRAM has two technology camps: the trench capacitor, which IBM champions, and the stacked capacitor, which NEC and TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) advocate. ISI is currently the sole supplier of commercial SOI floating-body-effect-memory IP. Other suppliers have R&D efforts under way. For example, Renesas (www.renesas.com) is developing an SOI floating-body-effect device, and Toshiba (www.toshiba.com) is working on both floating-body-effect memory and FERAM (ferroelectric RAM).

## TRENCH- VERSUS STACKED-CAPACITOR DRAM

IBM early on discovered the difficulties of combining DRAM with ASICs and labored through the 1990s with a one- to two-generation penalty in ASIC-logic performance when it combined ASICs with DRAM. IBM claims that this problem no longer occurs with its 130-nm and smaller process geometries (**Reference 4**). The company developed its Blue Gene/L supercomputer chip in 130-nm technology using embedded DRAM for the Level 3 cache. The company achieved 3.3-nsec, 300-MHz operation for the memory array, well within the design requirement of 250 MHz. Designers estimated that if they had fabricated the Level 3 in SRAM, it would have occupied 66% of the die. The area saving they achieved by using DRAM equated to a cost saving of 40%, without any compromise in performance.

The production of the trench capacitor is the first stage in wafer processing (**Figure 1**). The embedded DRAM follows the layout rules of the technology, and, after the deep trench processing, a planar wafer surface presents itself for designers to build the logic stages. Hence, the presence of the DRAM has minimal impact on the logic yield. The 130-nsec process requires four additional masks to implement the DRAM. IBM anticipates that future generations of embedded DRAM can achieve cycle times of less than 2.5 nsec and data rates of greater than 1.5 GHz and still maintain three- to four-times better density than SRAM.

NEC uses a stacked-memory architecture for its ML embedded DRAM with a zirconium-dioxide, high-K dielectric (**Reference 5**). This process includes an MIM (metal-insulator-metal) stacked capacitor to avoid the high-temperature process steps that conventional SIS (silicon-insulator-silicon) stacked DRAMs require (**Figure 2**). The low-temperature processing minimizes degradation of the logic performance and enables the DRAM to be compatible with standard logic CMOS, although this approach requires eight or nine additional masks.

The company is currently using a 90-nm process with a DRAM-cell size of 0.22 microns square and is moving toward 65- and 45-nm processes.

The difficulty with producing a stacked capacitor is that you must fabricate it in the middle of the process between the active devices and the wiring. Also, you must use novel materials to build the complex 3-D structure. Furthermore, additional planarizing steps are necessary to avoid the yield problems that would arise if metal tracks had to negotiate over tall capacitor structures. At a 90-nm process, NEC can incorporate as much as 256 Mbits of embedded DRAM on a 15×15-mm die; assuming that the memory occupies half the silicon area,

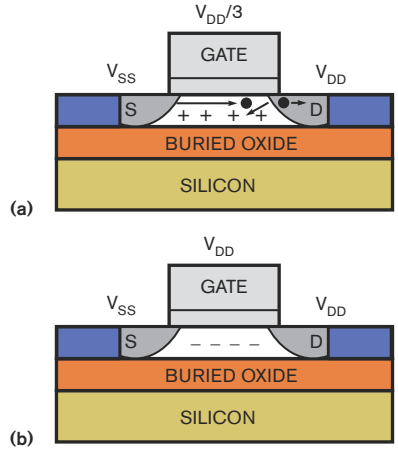
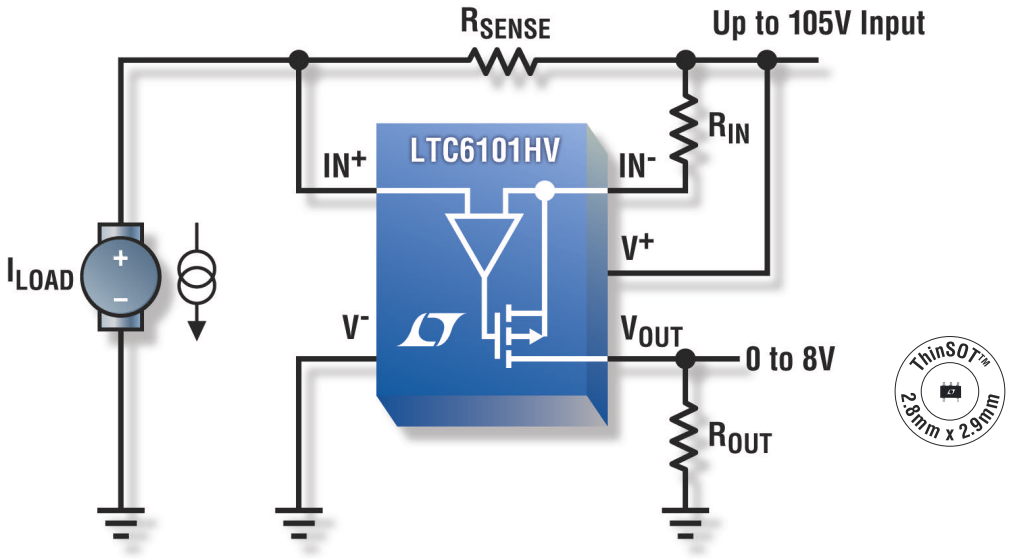



Figure 3 A floating-body-effect DRAM (a) stores information in the charge that becomes trapped in the body of an MOS SOI transistor (b).

# $I_{SENSE}$ to 105V

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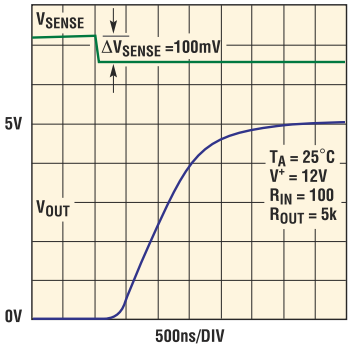


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## ANOTHER ALTERNATIVE

The issue confronting both the trench- and stacked-capacitor makers is that these capacitors are the final steps in an evolutionary path of 33 years that has taken them from planar capacitors in 8-micron technology to complex 3-D structures in 90-nm processes. The aspect ratio of these capacitors now exceeds 30-to-1, and the practical limit of fabricating capacitors in this way is looming. Floating-body DRAM, on the other hand, eliminates the need for a separate capacitor and provides a technology path that researchers have demonstrated experimentally at the 22-nm level (**Reference 6**).

Floating-body DRAM uses a MOS transistor instead of a capacitor to store each bit of data. The key point is that the memory employs an SOI wafer. Designers construct each transistor on its own silicon island and electrically isolate the transistors from one another, enabling each one to accumulate a charge. The quantity of this charge affects the current that flows through the transistor when you apply a voltage between the source and the drain (**Figure 3**). You can sense this difference in current and use it to indicate the storage of a one or a zero. To store a one in a cell, you apply the charge to the body of the transistor using impact ionization. This process is similar to the technique that flash memories employ, except that impact ionization is faster and uses less energy. Also, flash memories retain stored data for a long time, whereas Z-RAM loses its data after a few milliseconds if you do not refresh it. The much lower capacitance of the floating-body cell has additional implications. Because there is no bulk capacitance, drive and decoding circuitry can be faster. And the smaller capacitance means that refresh requires significantly less energy than with a capacitor-based DRAM.

Whereas each storage node in a conventional DRAM requires a capacitor and an access transistor, each node of a floating-body DRAM requires only one NMOS transistor. This simplicity enables the devices to achieve double the density of standard embedded DRAM at a 90-nm process, and this advantage will become greater at each succeeding process generation.

In January 2006, AMD endorsed floating-body-DRAM technology; the company subsequently licensed the IP from ISI to develop larger cache memories for its new generation of processors. "The agreement is part of our ongoing research into higher density and more energy-efficient on-chip memory," says an AMD spokesman. "We're looking at this technology for potential use in future AMD processors." Because AMD manufactures processors using SOI technology, floating-body DRAM as on-chip cache or working storage could be a natural fit, enabling the company to increase performance and reduce cost.

It is clear that embedded DRAM has a firm place in all application sectors. In consumer, communications, and automotive applications, a complex system ASIC with onboard DRAM may require no external memory at all. In computing applications, especially high-end processors, embedded DRAM enables the use of a large Level 3 cache, greatly increasing the memory bandwidth. IBM has followed this path with its Blue Gene/L supercomputer chip, and AMD will likely follow, bringing L3 cache into the PC market. The final determinant is technology. SOI processing is quickly moving into the mainstream. It is a case of simple arithmetic to demonstrate that the combination of SOI and embedded floating-body DRAM produces the most economic high-performance ASIC technology. EDN

## AUTHOR'S BIOGRAPHY

*Raymond Ambrose operates Randa Creative (www.randacreative.com), which he founded in 2005 after 33 years in electronics. The first 10 of those years, he worked in telecom, and the last 23, he worked in microelectronics for STMicroelectronics, where he managed the development of high-end graphics accelerators and contributed to the development of digital-satellite television. Ambrose also writes technical articles for the electronics industry and is a photographer, specializing in microphotography of electronic components. You can reach him at ray.ambrose@randacreative.com.*

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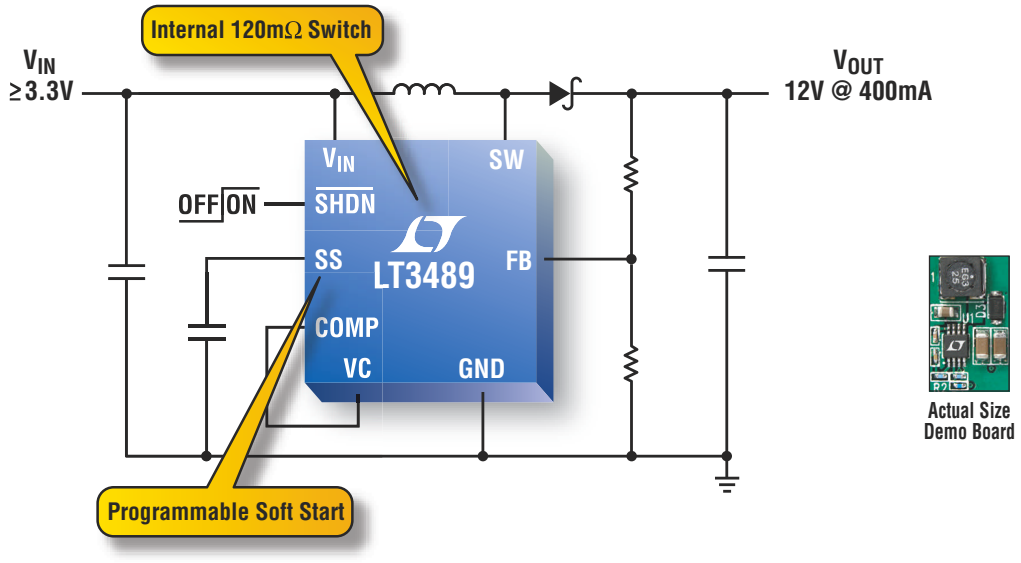




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| LT3477 | 2.5V to 25V | 40.0V | 3A | 3.5MHz | 4mm x 4mm QFN-20, TSSOP-20E |
| LT3479 | 2.5V to 24V | 40.0V | 3A | 3.5MHz | 4mm x 3mm DFN-14 TSSOP-16E |
| LT1370HV | 2.7V to 30V | 40.0V | 6A | 500kHz | TO-220, TO-263 |

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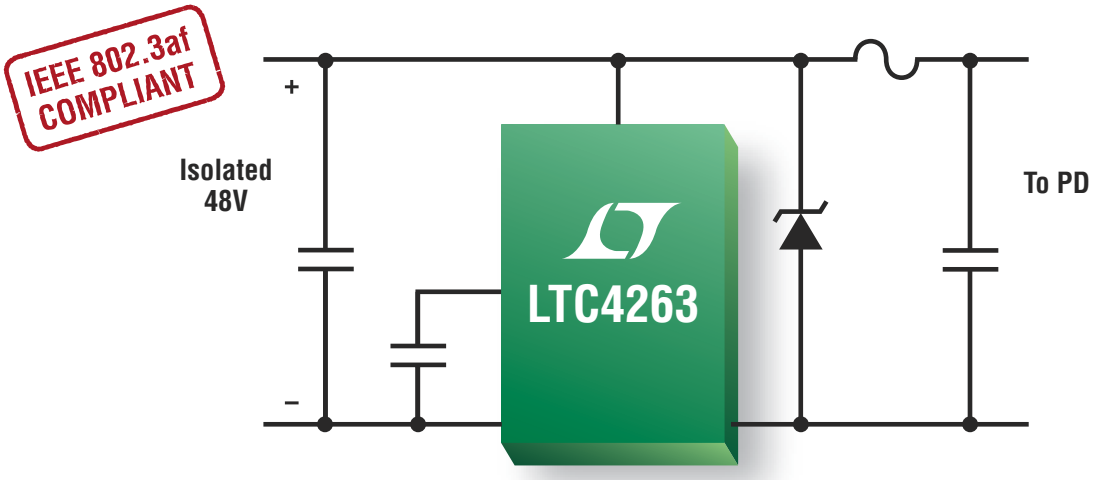


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- Powered Device (PD) Detection and Classification
- LTC4263: $2.95 each in 1k qty

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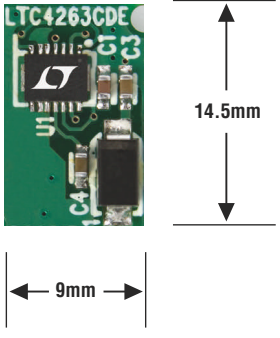


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EDITED BY BRAD THOMPSON
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# designideas

READERS SOLVE DESIGN PROBLEMS

## Two-channel audio amplifier drives stepper motor

Phill Leyva and Bill Quach, Maxim Integrated Products, Sunnyvale, CA

Although relatively expensive, monofilar-wound, bipolar stepper motors provide strong torque for a given physical size. However, each of the motor's two windings requires eight driving transistors connected in groups of four in an H-bridge configuration. Each transistor must withstand and quickly recover from overloads and short-circuit conditions, and a driver must consequently include complex and large discrete-component protective circuitry.

As an alternative, **Figure 1** shows a motor-driver circuit based on Maxim's (www.maxim-ic.com) MAX9715, a tiny, surface-mount, 2.8W Class D audio amplifier, which typically drives 4 or 8Ω speakers. Each of $IC_1$'s two outputs consists of a MOSFET H-bridge that drives a pair of output lines, OUTR+ and OUTR− and OUTL+ and OUTL−, that connect to the stepper motor's A and B windings, respectively. Each pair delivers a differential-pulse-width-modulated signal with a nominal switching frequency of 1.22 MHz. The circuit's low-interference design eliminates the requirement for output-line filters.

Capacitors $C_1$, $C_3$, $C_4$, and $C_6$ provide bypassing for $IC_1$'s power input and bias pins, and $C_5$ and $C_7$ provide bulk-holdup capacitance for the Class D power amplifiers' outputs. Capacitors $C_8$ and $C_9$ limit the amplifiers' input bandwidth to 16 Hz, and $L_2$ and $L_3$ suppress electrical-noise pickup by the long input cables. Comprising $C_1$, $C_2$, and ferrite bead $L_1$, a pi-section noise filter suppresses noise on $IC_1$'s power-sup-

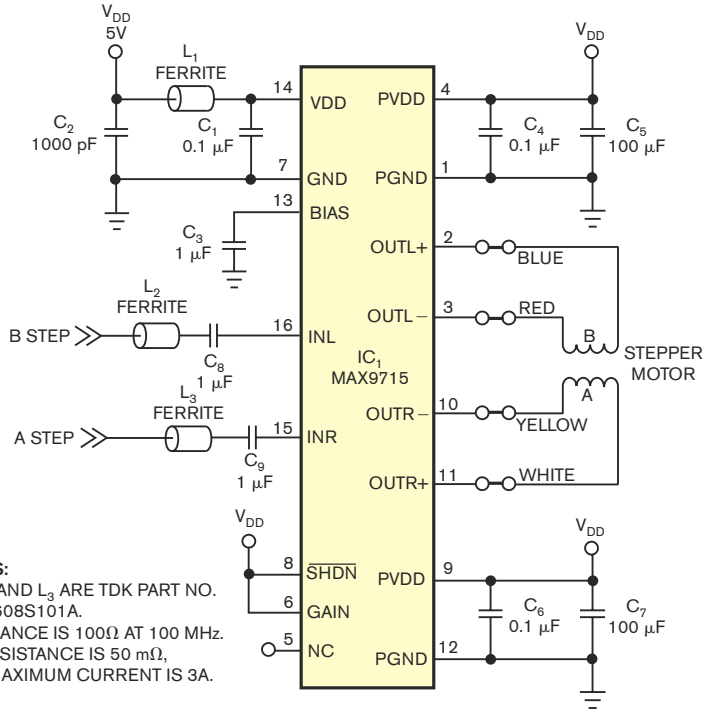


Figure 1 A single surface-mount circuit and a few passive components can drive a bipolar, monofilar-wound stepper motor.

### DIs Inside



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TABLE 1 A_STEP AND B_STEP PULSE SEQUENCE

| Step | A_Step | B_Step |
|---|---|---|
| 0 | H | L |
| 1 | L | L |
| 2 | L | H |
| 3 | H | H |
| 4 | H | L |

ply input. A suitable controller feeds digital pulses to $IC_1$'s A_Step and B_Step inputs, which respectively drive the motor's right and left channels. Internal short-circuit and thermal protection guards the amplifier against overcurrent and short circuits caused by the stepper motor or its connecting leads.

**Table 1** illustrates the A_Step and B_Step pulse sequence that rotates a typical stepper motor in one direction by continuous application of steps 0 through 4. Step 4 returns the motor's shaft to its starting position and completes its 360° rotation. To reverse the motor, begin at the bottom of the **table** to reverse the pulse pattern and work upward. You can disable both of the amplifier's channels by applying a logic-low signal to Pin 8, $IC_1$'s active-low $\overline{SHDN}$ input. **Figure 2** illustrates the circuit's input and output waveforms. EDN

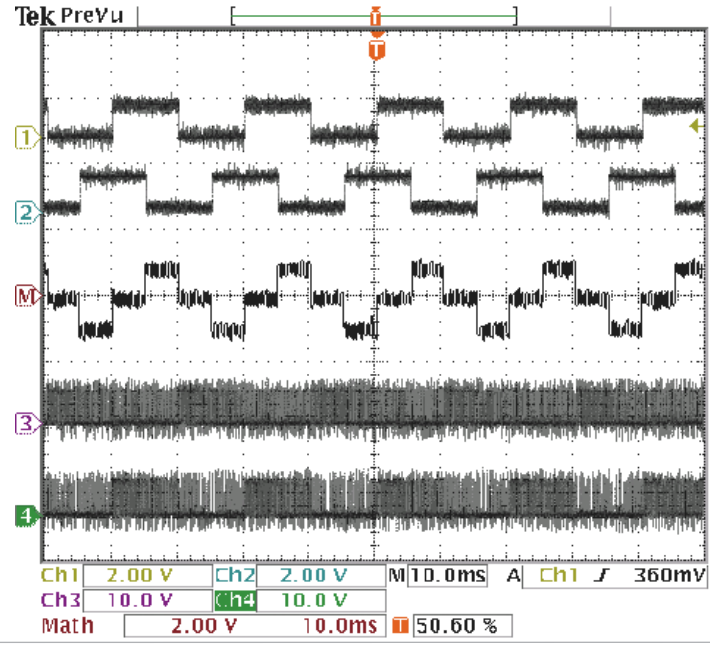


Figure 2 Waveforms from the circuit in Figure 1 include the A_Step input (Channel 1), B_Step input (Channel 2), outputs OUTR+ (Channel 3) and OUTR− (Channel 4), and the signal that arrives at the motor's windings (OUTR+ minus OUTR−, middle trace), which the oscilloscope's math function computes.

# Get power from a telephone line without disturbing it

Yongping Xia, Navcom Technology, Torrance, CA

An idle telephone line tempts designers to use its 48V potential as a power source. However, Part 68 of the US Federal Communications Commission's telecommunications regulations states that any device that connects to the phone line and is not actively communicating must present a resistance of at least 5 MΩ (**Reference 1**). To meet this requirement, a device's continuous-current drain must not exceed 10 µA. Fortunately, many devices that connect to the phone line do not require continuous power and can remain off for long intervals, awakening only for a short time before relapsing into power-off mode. Providing power for these applications from the phone line presents obvious advantages by eliminating the need for a battery or another power source and the cost of battery maintenance.

The circuit in **Figure 1** charges a 1.5F supercapacitor, $C_1$, from the phone line through a diode bridge and a 5.6-MΩ resistor. A Maxim (www.maxim-ic.com) MAX917 nanopower comparator, $IC_1$, consumes only 0.75 µA from its power supply. Resistors

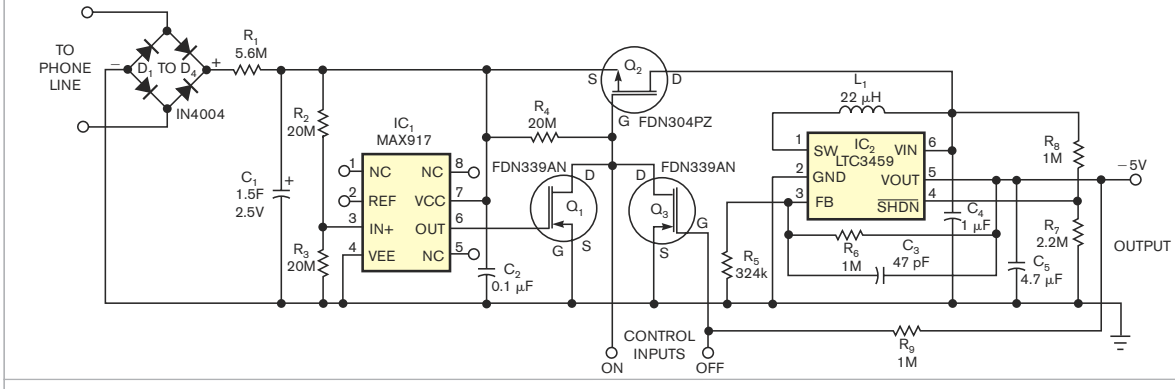


Figure 1 This power-conversion circuit delivers intermittent bursts of regulated voltage from a supercapacitor charged by a trickle of current from a telephone line.

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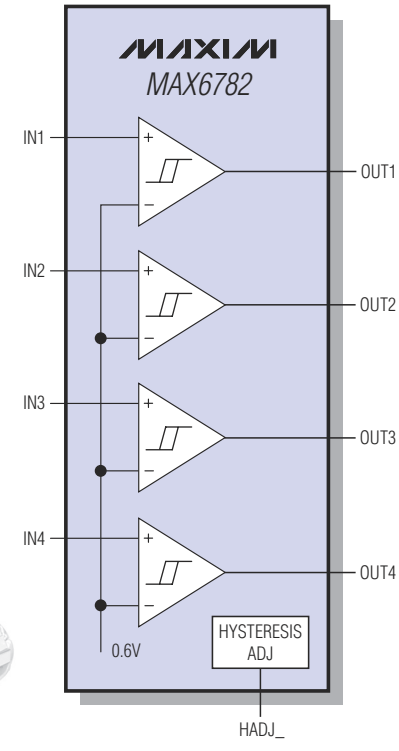
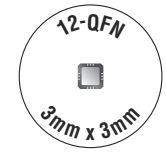



| Part | Voltages Monitored | Monitoring Configuration | Package |
|---|---|---|---|
| MAX6782/MAX6783 | Quad | UV | TQFN (3mm x 3mm) |
| MAX6784/MAX6785 | Triple | UV | |
| MAX6786/MAX6787/MAX6788 | Dual | UV | |
| MAX6789/MAX6790 | Quad | OV | |
| MAX6775/MAX6776/MAX6777 | Single | UV | SC70/µDFN |
| MAX6778/MAX6779/MAX6781 | Dual | UV | |

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$R_2$ and $R_3$ halve the voltage across $C_1$ and apply it to $IC_1$'s positive input voltage at Pin 3 for comparison with its built-in 1.245V reference. For voltages across $C_1$ that do not exceed 2.49V, $IC_1$'s output at Pin 6 remains low. When $C_1$'s voltage reaches 2.5V, Pin 3's voltage exceeds the reference voltage, and $IC_1$'s output goes high, turning on $Q_1$ and $Q_2$.

Several days must elapse before $C_1$ becomes fully charged, given its huge capacitance and a charging current of less than 10 µA. The voltage on $C_1$ can never exceed 2.5V because, once it reaches 2.49V, $Q_1$ and $Q_2$ turn on, connecting $C_1$ to a switched-mode-power-supply circuit. Because the power-supply current exceeds the charging current, the voltage across $C_1$ starts to decrease when $Q_2$ turns on. Transistor $Q_3$ holds $Q_2$ on when $C_1$'s decreasing voltage causes $Q_1$ to turn off.

The switched-mode-power-supply circuit comprises a Linear Technology (www.linear.com) LTC3459 micropower boost converter, $IC_2$, and its associated components, which deliver 5V at 10 mA. A fully charged $C_1$ can supply power to a 10-mA load for approximately 40 sec. With no load, the circuit can sustain its 5V output for more than 10 hours. For greater output current and shorter operating time, select another boost converter that can operate at a low input voltage.

Mechanical switches, open-drain MOSFETs, open-collector transistors, or a microcontroller's open-drain output pins can drive two external control inputs to force the circuit on and off. Pulling the On input low forces $Q_2$ to turn on and deliver power from $C_1$ to the power converter, and pulling the Off input low turns off $Q_2$ and removes power from the converter. Note that the power converter's output-return line connects to the telephone line and thus should not connect to an earth ground or to grounded equipment. EDN

## REFERENCE

1 "Part 68," Federal Communications Commission, www.fcc.gov/wcb/iatd/part_68.html.

# Active-filter circuit and oscilloscope inspect a Class D amplifier's output

John Guy, Maxim Integrated Products Inc, Sunnyvale, CA

The increasing acceptance of Class D amplifiers has helped them gain market share from their linear Class AB brethren. That acceptance is no surprise; the advantages of Class D amplifiers are legion, but such amplifiers also require new techniques for evaluation. For example, consider a basic sine-wave test of a linear amplifier. You apply power, apply a sine wave of suitable amplitude to the input, and connect an oscilloscope probe to the output. You'll see a replica of the input, usually offset by about half the power-

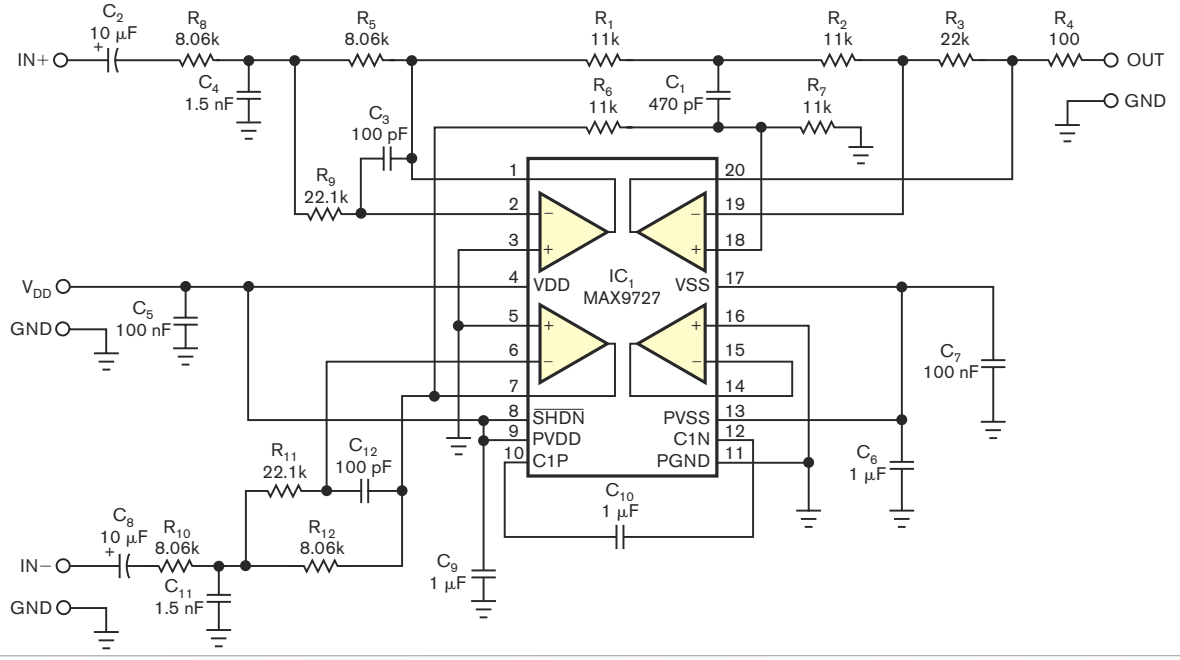


Figure 1 Use this third-order, 30-kHz filter circuit to observe a Class D amplifier's output signal on an oscilloscope.

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supply voltage. Even if the linear amplifier drives a BTL (bridge-tied load), you'll still see a recognizable replica of the input at either end of the load, albeit at half of the output signal that's available.

Testing a Class D amplifier poses more difficulties. The amplifier's output comprises a PWM (pulse-width-modulated) signal that swings between ground and the supply voltage at a frequency that's usually 200 kHz to 2 MHz. However, when you view this PWM output on an oscilloscope, you'll see no resemblance to the sine-wave input.

You can observe a Class D audio amplifier's output if you introduce the filter circuit in **Figure 1**. Based on Maxim's (www.maxim-ic.com) MAX-9727 quad-audio-line driver, $IC_1$, the circuit combines separate single-ended filters—one for each of the BTL outputs' phases—with a third amplifier that provides a difference signal with additional filtering. The first stage of each single-ended-filter section contributes the complex-conjugate pole pair of a third-order, 30-kHz multiple-feedback Butterworth filter, for which many design guidelines and equations are available. Each third-order-filter section comprises a complex-conjugate pole-zero pair and one real pole.

To improve the match between the signal paths, the two separate multiple-feedback filters share a real pole, which 470-pF capacitor $C_1$ and 11-kΩ resistors $R_1$ and $R_6$ provide. The circuit implements that pole as a difference amplifier, thereby producing a filtered output that presents a single-ended version of the BTL amplifier's outputs. The filters' signal paths present 5.5-kΩ impedances to each of the A and B amplifier sections' inputs. By inspection, the net 5.5-kΩ impedance from Section B's output to $C_1$ comprises the Thevenin-equivalent impedance of resistors $R_6$ and $R_7$. Similarly, the net impedance from Section A's output to $C_1$, also 5.5 kΩ, comprises the Thevenin impedance of resistors $R_1$ and $R_2$. Note that the virtual ground from Amplifier D's inverting input effectively grounds resistor $R_2$.

Matched resistors attenuate each of Amplifier D's differential inputs by 6 dB (IN+ by $R_1$ and $R_2$ and IN− by $R_6$ and $R_7$). A 22-kΩ feedback resistor, $R_3$, provides Amplifier D with a gain of two, which sets a unity-gain-transfer function in the circuit's passband. The circuit's single-ended output with respect to ground allows the oscilloscope's ground to also serve as the output signal's ground. A version of this circuit using conventional op amps would require a negative-power-supply-voltage source, but Maxim's MAX9727 already includes a negative-voltage source, which its internal charge-pump circuit generates. When you operate the circuit from a 5V supply, the circuit's output delivers more than 2.5V rms. Although its third-order filter is inadequate for precise measurements of distortion or noise, the circuit provides an excellent tool for troubleshooting and evaluating Class D-amplifier circuits and inspecting their outputs on an oscilloscope. EDN

# Voltage-to-pulse-width converter spares microprocessor's resources

James Christensen, Kris Design Co, El Cajon, CA

Although not an ADC in the classic "stream-of-ones-and zeros" sense, this voltage-to-pulse-width converter produces a logic-level output pulse whose variable width represents an analog of the input voltage. Based on Atmel's (www.atmel.com) AT89LP4052 microprocessor, $IC_1$, this circuit makes efficient use of the target microprocessor's limited analog-port pinout and code space by using a modified version of the classic timed-discharge-RC (resistor-capacitor) ADC design.

The timed-RC ADC allows a capacitor to charge through a resistor while the microprocessor increments a counter. When a comparator detects that the capacitor voltage and analog- input voltage are equal, the count terminates, and its stored value represents the ADC's output. However, an RC network's exponential charging characteristic produces a nonlinear conversion. Various software and hardware techniques can partially correct the nonlinearities, but all entail adding code, increasing the circuit's development time, or consuming additional I/O-port pins required for other purposes.

To produce a linear-charging characteristic that needs no correction, the circuit in **Figure 1** uses an LM334 constant-current source, $IC_2$, to drive capacitor $C_2$, which connects to $IC_1$'s $AIN_0$ analog-input port. An internal timer in the microcontroller measures the elapsed time from the charging ramp's start to the instant when the ramp voltage crosses the analog-input-voltage threshold at $IC_1$'s $AIN_1$ port.

In this application, potentiometer $RV_1$ provides an analog-input voltage proportional to its position. The width of the positive-going pulse at the output, P1.5, varies in proportion to the analog-voltage input. Note that I/O-port pin $AIN_1$ serves a dual purpose as an analog input and as an open-drain output that discharges ramp-forming capacitor $C_2$ before the next conversion cycle.

An 8-bit voltage-to-pulse-width-conversion cycle completes in less than 4 msec. The code performs the conversion function and outputs a pulse train at $IC_1$'s port P1.5 (Pin 17) with a period of 100 msec and a positive-going pulse width proportional to the analog-input voltage at Pin 13 ($AIN_1$). Programming connector $J_1$ provides access to $IC_1$ for

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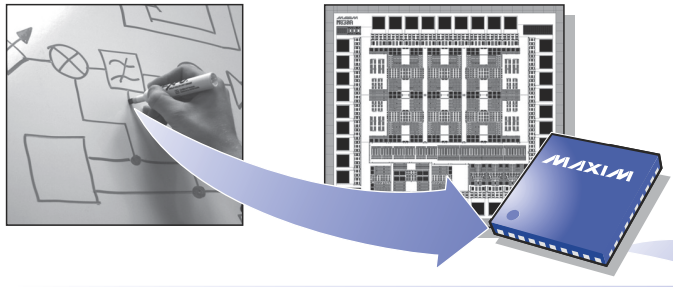


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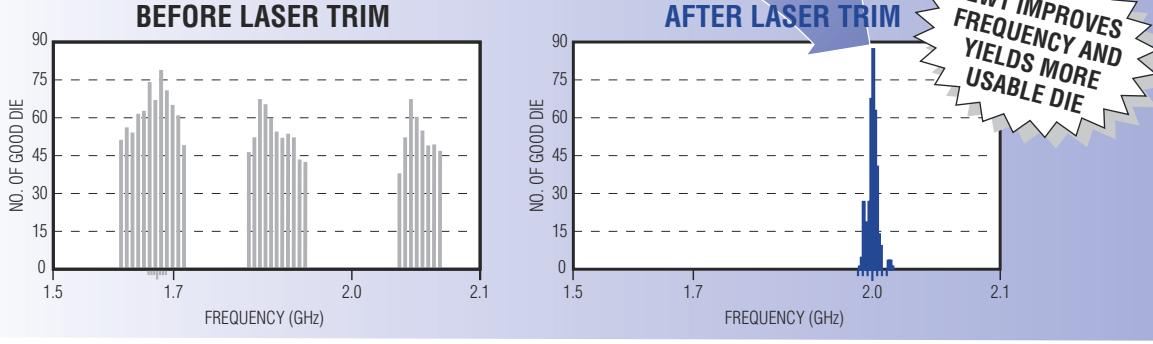


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uploading the compiled code. The AT89LP4052 microprocessor typically executes one instruction per clock cycle, and a 10-µsec timer routine can perform the required housekeeping functions with plenty of time left over for other program tasks, including a future application that requires a binary-coded analog-to-digital output. You can download **Listing 1**, which is written in C for the Keil Software (www.keil.com) compiler, from the online version of this Design Idea at www.edn.com/061201di1.EDN

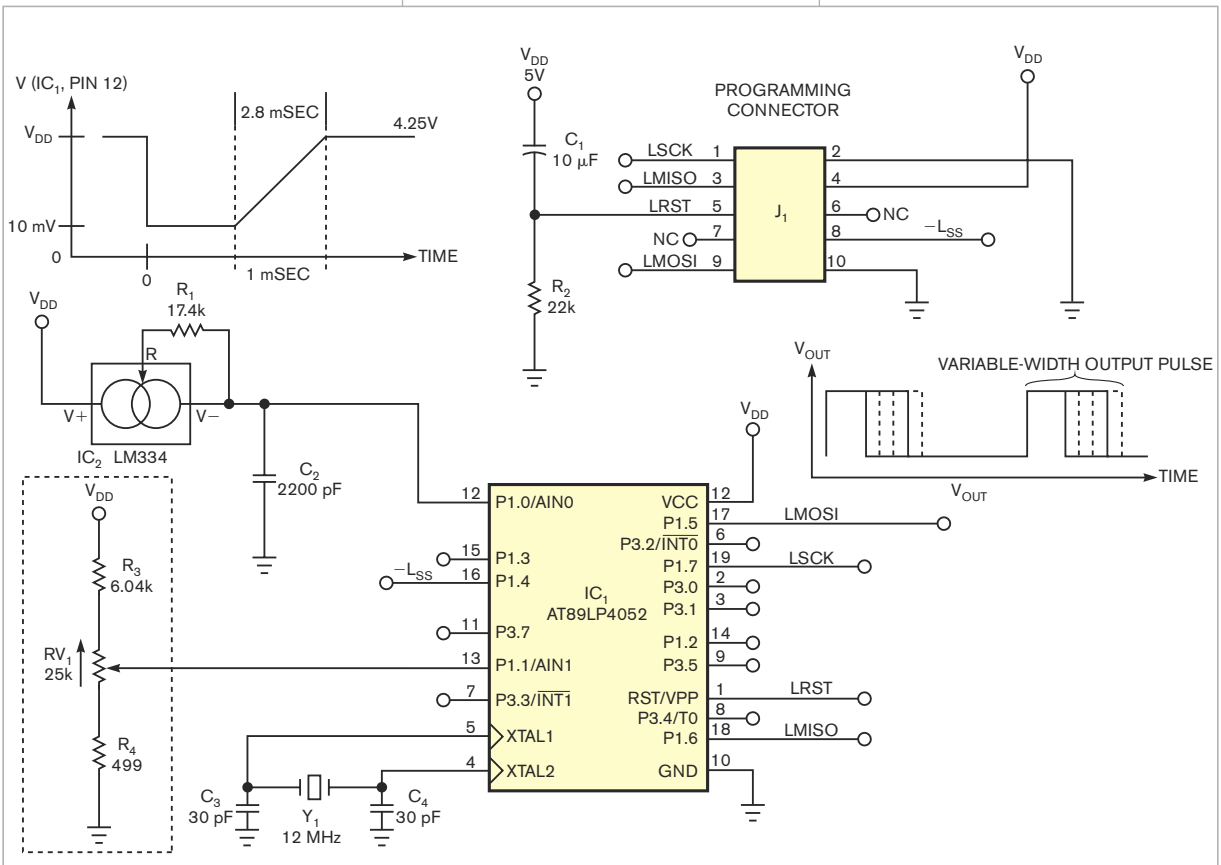


Figure 1 An analog-voltage-to-pulse-width converter features minimal parts. Subgraphs show timing-network and output-voltage waveforms. $IC_1$'s unlabeled pins are available for user functions.

# Precision voltage reference delivers 80 mA

James Horste and Gary Staiman,
Maxim Integrated Products Inc, Sunnyvale, CA

Large analog systems that present many loads to a voltage-reference source can often demand more current than a single reference IC can deliver. However, if the reference IC includes force and sense terminals, you can easily add a buffer to the circuit's feedback loop without affecting the reference's accuracy. For example, the circuit in **Figure 1** provides the same 0.04% initial accuracy and 7-ppm/°C temperature coefficient as $IC_1$, a standalone MAX6033. The buffer circuit delivers as much as 80 mA.

When you design a buffer stage for a force/sense-control loop, the buffer must provide unity-voltage gain with no phase inversion. In addition, the circuit's power supply must provide head-room voltage to accommodate the reference voltage plus voltage drop across the buffer stage. The simplest buffer circuit comprises an NPN transistor that connects as an emitter follower, which requires a drive voltage that exceeds the reference's output voltage by one transistor base-

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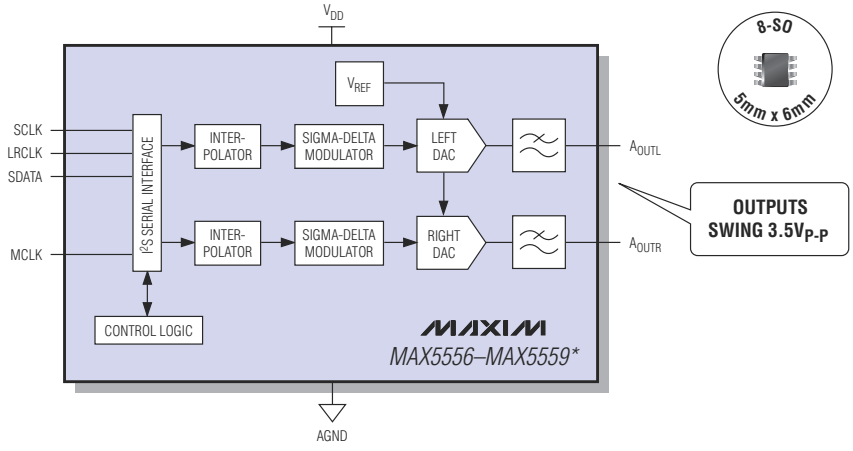





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emitter voltage drop. If you add the required minimum power-supply voltage plus the maximum allowable base-emitter voltage, the configuration runs out of head room. Using a PNP stage to drive the emitter drive stage solves the head-room problem but inverts the output voltage and prevents the force/sense loop from functioning. Adding a second PNP stage cancels the phase inversion but destabilizes the force/sense loop by adding excessive gain.

The modified complementary Darlington, or Sziklai, connection (**Reference 1**) in **Figure 1** solves both problems by providing an emitter follower's unity-voltage gain with no inversion. The output PNP stage provides plenty of head room, but the NPN stage does not. You can easily overcome this drawback by adding diode $D_1$ to shift the NPN transistor's emitter voltage downward by a diode drop. Thus, to a first approximation, the diode's voltage drop and the transistor's base-emitter voltage cancel one another, leaving plenty of voltage head room.

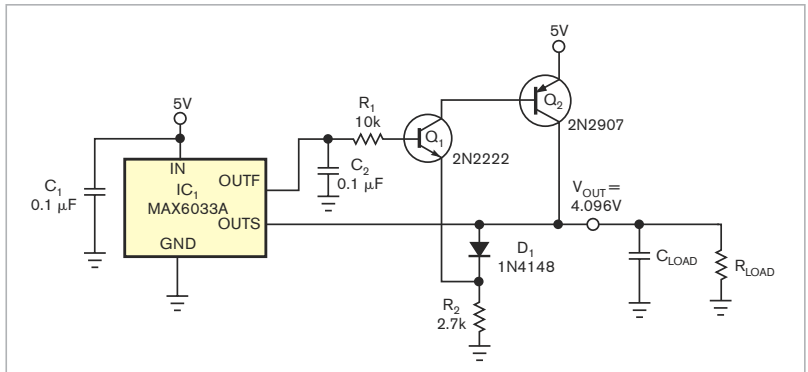


Figure 1 Add a two-transistor output buffer to a 4.096V, 15-mA reference IC to boost its output current to 80 mA or higher.

Transistor $Q_2$, a 2N2907, provides limited current gain, which in turn limits the circuit's maximum output current to 80 mA. Substituting a higher gain transistor can increase the output current to any reasonable level.

For stability, the MAX6033 requires 0.1-µF ceramic bypass capacitors on its In and OutF pins. Capacitor $C_2$ determines the circuit's response speed, but the buffer circuit exerts no significant effect on transient response. Most dc-reference-voltage ICs cannot accommodate a fast-changing load-current step; thus, the circuit's transient response and its ability to supply fast current spikes depend on the output capacitor, $C_{LOAD}$. Values of $C_{LOAD}$ as high as 10 µF do not affect the circuit's stability. EDN

## REFERENCE

1 "Sziklai Pair," Wikipedia, http://en.wikipedia.org/wiki/Sziklai_pair.

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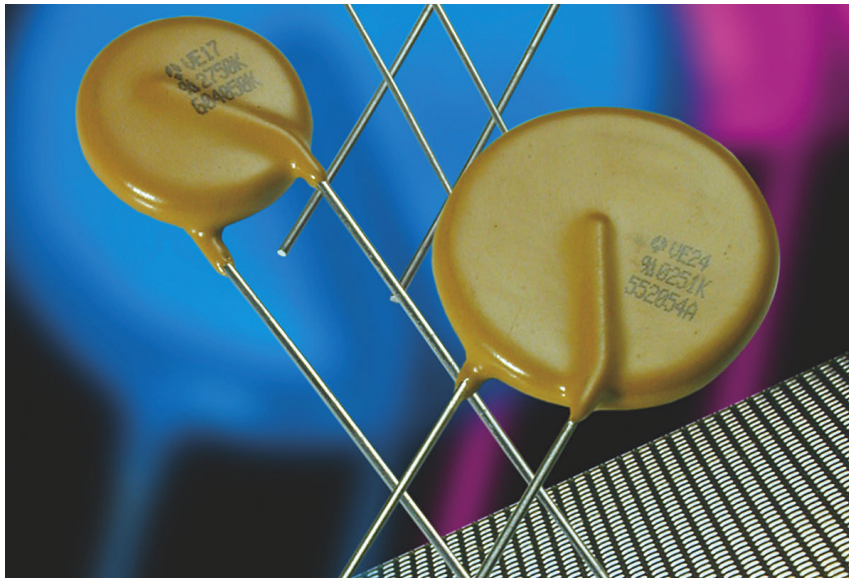
# productroundup

## PASSIVES



### ROHS-compliant MOVs provide transient-voltage protection

Joining the vendor's VE/VF series MOVs (metal-oxide varistors), the new devices feature a lead-free version. These ROHS (restriction-of-hazardous-substances)-compliant units provide transient-voltage protection by limiting surge voltages and absorbing energy pulses. Features include an 18 to 825V-dc operating-voltage range, 0.4 to 230J energy absorption, and 10,000A peak-current handling. The MOVs costs 4 cents each (10,000).
**AVX Corp, www.avx.com**

### Thick-film chip resistors handle 2W of power

Capable of handling 2W of power, the thick-film RHC series SMD chip resistors achieve 1 and 5% tolerances at a TCR (temperature coefficient of resistance) of 100 ppm. Features include E24 values of 0.1Ω to 1 MΩ and a 200V continuous-working voltage. A significantly larger bottom termination provides more reliable termination with improved heat conduction. Available in a 2512 size, the RHC units cost 12 cents each (4000) for 5% tolerance and 18 cents for 1% tolerance.


**Stackpole Electronics, www.seielect.com**

### High-current inductor keeps a low profile

Adding to the vendor's low-profile, high-current IHLP inductor family, the IHLP2525CZ11 inductor has a 1- to 22-µH inductance range with a ±20% inductance tolerance. Features include a 2.5 to 9.5A saturation-current range, a 7.6- to 128.9-mΩ typical dc-resistance value and an 8- to 135-mΩ maximum dc-resistance value. Measuring 6.47×6.86 mm, the device has a 3-mm-high profile. Available in a 2525 footprint, the IHLP2525CZ11 inductor costs 32 cents (10,000).
**Vishay, www.vishay.com**

### Voltage-divider network is ROHS-compliant

Extending the resistance range from 5 to 100 kΩ to 1 to 100 kΩ, the SS1 series networks have a 100V-dc maximum operating voltage. The ROHS (restriction-of-hazardous-substances)-compliant voltage-divider network includes R2/R1 ratio values, including 10, 9, 4, 3, 2, and 1, with a ±0.05% ratio tolerance and a ±5-ppm/°C TCR (temperature coefficient of resistance) tracking tolerance. Available in an SOT-23 package, the SS1 series is available at prices of 30 to 40 cents (10,000).

**BI Technologies, www.bitechnologies.com**

### Wirewound power-inductor series comes in 13 models

Targeting dc/dc-converter-choke-coil applications, the wirewound NR8040T series power inductors suit LCD and plasma TVs, automobile-navigation systems, home-video-game consoles, and other devices. The series features 13 models offering a 0.006 to 0.29Ω dc-resistance range, a 0.9- to 100-µH inductance range, and a 1 to 11.8A

LINEAR TECHNOLOGY

DESIGN NOTES

# Dual Monolithic Step-Down Switching Regulator Provides 1.6A Outputs with Reduced EMI and $V_{OUT}$ as Low as 0.8V

Design Note 404

Hua (Walker) Bai

## Introduction

Electronic devices are becoming smaller while the power requirements are increasing to satisfy ever more functionality. To preserve power and manage heat, switching regulators are desirable because of their high efficiency compared to linear regulators.

The LT3506 and the LT3506A are examples of how to squeeze power out of a supply without overheating the end product. These are dual 1.6A step-down monolithic regulators that simplify the lives of system engineers. They eliminate the need for external power switches, thereby reducing solution size and BOM cost. Their outputs can be as low as 0.8V, satisfying the needs of the latest DSPs. Integrated dual output channels reduce the part count, while anti-phase switching of the two channels maximizes efficiency and reduces input current ripple and EMI. Both the LT3506 and the LT3506A have 0.8V high accuracy voltage references.

## Typical LT3506A and LT3506 Applications

The primary difference between the LT3506A and the LT3506 is the switching frequency. The LT3506A's switching frequency is 1.1MHz while the LT3506's is 575kHz. Higher switching frequency allows smaller components. For lower output voltages, i.e., less than 3.3V, the LT3506 is recommended if $V_{OUT}/V_{IN(MAX)}$ is less than 15%. The lower switching frequency option usually results in higher efficiency due to the lower switching and inductor core losses.

The circuit in Figure 1 generates a 3.3V and a 5V output. The overall efficiency of the circuit (both channels) is shown in Figure 2. The circuit shown in Figure 3 generates a 1.2V and a 1.8V from a 3.6V to 21V input. The wide input voltage of both the LT3506 and the LT3506A (3.6V to 25V) can accept a variety of power sources, from lead-acid batteries and 5V rails to unregulated wall adapters and distributed power supplies.



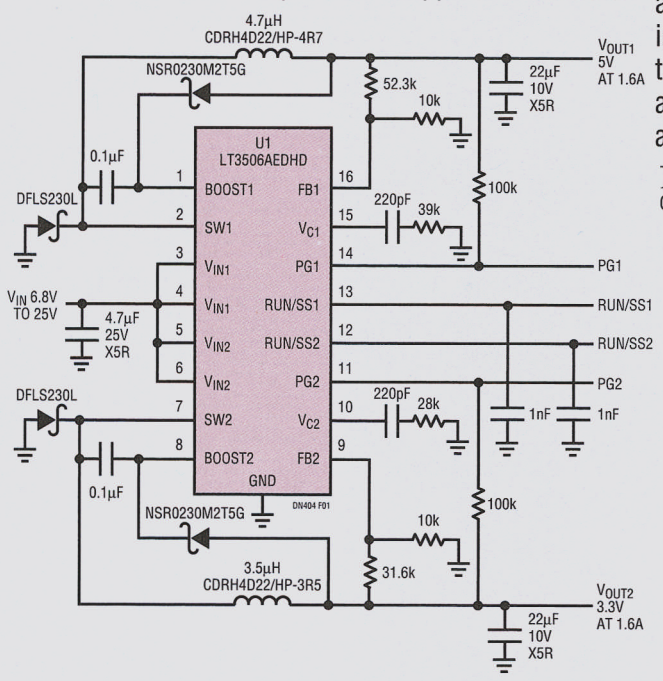



**Figure 1. LT3506A Application Circuit Provides Dual Outputs of 5V at 1.6A and 3.3V at 1.6A**

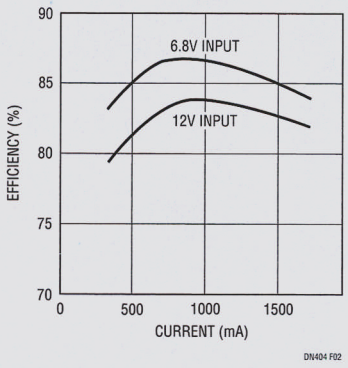



**Figure 2. Overall Circuit Efficiency (Both Outputs Loaded Identically)**

The LT3506's high switching frequencies allow the use of small, low profile surface mount inductors and ceramic capacitors, resulting in smaller solution size and lower assembly cost. Furthermore, the low ESR of ceramic capacitors and high switching frequency results in very low, predictable output voltage ripple.

The internal supplies of both the LT3506 and LT3506A are powered from $V_{IN1}$ pins. It is possible to supply power via the $V_{IN2}$ pin from a different source, or it can be simply tied to $V_{OUT1}$, provided $V_{OUT1}$ can supply sufficient current. The efficiency of $V_{OUT2}$ can be improved when supplying $V_{IN2}$ from a separate, lower supply voltage. Cascading $V_{IN2}$ to $V_{OUT1}$ also enables some low duty cycle applications for $V_{OUT2}$.

The thermally enhanced 16-lead DFN or TSSOP packages have an exposed ground pad on the bottom. This ground must be soldered to a ground pad on the PCB. Adding a dozen thermal vias to this pad improves thermal performance. A higher temperature grade part, I-grade, is also available.

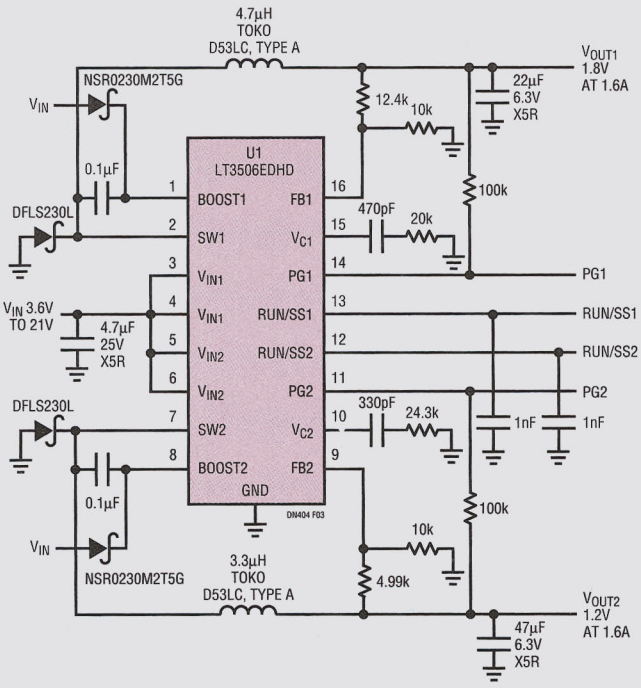



**Figure 3. LT3506 Application Circuit Provides Dual Outputs of 1.8V at 1.6A and 1.2V at 1.6A**

## Power Sequencing without Adding Components

Supply sequencing is critical in many systems in order to prevent possible latch-up and to improve system reliability. Independent PG (Power Good) indicators, RUN/SS pins and $V_C$ pins of the LT3506 and the LT3506A simplify supply sequencing. The PG pin remains low until the FB pin is within 10% of the final regulated output voltage. The easiest way to sequence outputs is to tie the PG1 pin to the $V_{C2}$ pin. Then remove the pull-up resistor on PG1. This enables $V_{OUT1}$ to come up before $V_{OUT2}$ as shown in Figure 4.

## 2-Phase Switching Eases EMI Concerns

A step-down switching regulator draws current from its input supply and its input capacitor, resulting in a large AC current that can generate EMI. The LT3506's two regulators are synchronized to a single oscillator and switch out of phase by 180 degrees. Compared with two completely independent regulators, the input current ripple of the LT3506 is substantially reduced and its effective frequency doubled, thereby lowering EMI and allowing the use of a smaller input capacitor without reducing efficiency.

## Conclusion

Both the LT3506 and LT3506A step down the output voltage to as low as 0.8V and provide 1.6A of current capability per channel. 2-channel anti-phase switching substantially reduces the input current ripple and eases EMI concerns. The PG, $V_C$, and RUN/SS pins make supply sequencing simple and straightforward. Two package options (leadless and leaded) and two switching frequency options allow optimal solutions for most applications.

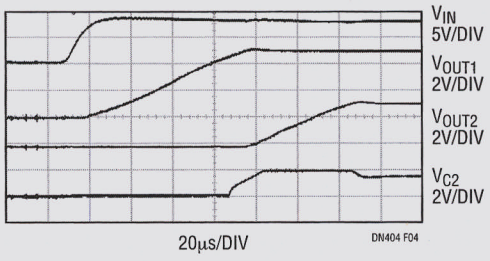



**Figure 4. Start-Up Waveforms of the Circuit in Figure 1 with Power Sequencing**

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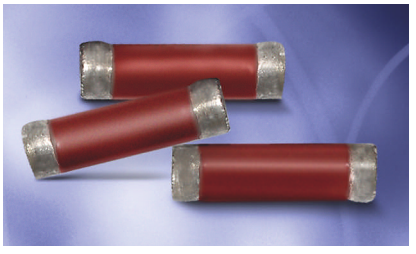
# PASSIVES

current rating. The NR8040T-100M device provides a 3.4A current at 10 µH. Available in an 8×8×4-mm package, the NR804T series costs 30 cents.
**Taiyo Yuden, www.yuden.us**

## Resistors target surge/pulse and thermal-cycling applications

Targeting circuits subject to extreme thermal cycling, the rugged, cylindrical surface-mount HSF and SMC series resistors suit surge/pulse and thermal-cycling applications. The HSF series features a 1W power rating at 70°C and a 350V working voltage. The units feature 5.9, 11, 27, 68, and 270Ω resistances; ±10% tolerance; and ±50 ppm/°C TCR (temperature coefficient of resistance). The SMC series has a



1W power rating at 70°C for the 2512 package and a 2W power rating at 70°C for the 3610 package. Resistance ranges from 1 to 2 MΩ, with a ±5% tolerance and ±50 ppm/°C TCR. Providing maximum thermal compliance, the SMC series features metal caps fitted on the terminals of the cylindrical resistor body. This technique provides improved thermal compliance, relieving stresses created from the TCE (thermal-coefficient-of-expansion) mismatch between the ceramic component and the FR4 pc board. The HSF and SMC series resistors cost 18 cents each.
**IRC, www.irctt.com**

# EDA TOOLS

## Power-analysis tool improves clock gating and clock tracing

The newest version of the PowerTheater RTL power-estimation and -management tool, the PowerTheater65 improves clock-gating, clock-tracing, and clock-power-reporting capabilities. Improved hierarchical-clock gating allows users to better determine where they should place integrated clock-gating cells and applies to common clocks and enable signals across hierarchical boundaries. This tool also reports on the number of registers gated in a design. The clock-tracing algorithms and tracing-distribution networks use combinational and sequential timing arcs in the timing libraries, assisting designers in guide-clock tracing. These tools also generate a clock-domain-tracing report, showing the power of all elements the tool has traced in the clock domain. A clock-enable-condition power linter determines the effectiveness of the clock by analyzing the relationship between the clock-enable signal, the clock signal, and the data signal for inferred registers in the design. The power-analysis tool extends support to the gate-level vectorless power estimation and can now read encrypted Liberty (synlib) format libraries. The PowerTheater65 costs $175,000 for a three-year time-based license.
**Sequence Design, www.sequencedesign.com**

## Vendor adds features to its SiP Analysis suite

Adding IC/package/pc-board co-design-analysis features to the vendor's SiP (system-in-package) Analysis suite allows the tool to better model power across the IC, package, and pc board. The PakSi-E tool generates a CPP (chip-package-protocol) package model that automatically maps ports between the IC design's Spice deck and package model. Apache Design's (www.apache-da.com) RedHawk static and dynamic IC power tool can read this model, allowing IC designers to search for power problems and their impact on timing across the combined IC and package. The vendor has also added features to the PowerGrid tool, merging single-chip packages or SiP geometry with a pc-board geometry. This approach allows users to identify hot spots on the pc board and package or SiP on which current and frequency are pooling and can cause failures. Prices for the SiP Analysis suite start at $65,000.
**Optimal Corp, www.optimalcorp.com**

## Wire-harness upgrade adds design-managing features

Targeting the design of wire harnesses in planes, trains, and automobiles, the Capital HarnessXC features Internet-based integration technologies and a data-driven graphical-styling engine. The engine allows designers to work with common tools and processes across multiple locations. New features include the embedded change-policy manager, allowing designers to configure how to evaluate and apply design changes, and an intelligent-styling capability, allowing designers to configure standards and ensure that they ren-

## EDA TOOLS

der drawings based on the specified design data and graphical standards. Additional features include data reporting and drawing access through direct links with MCAD packages, including CATIA Version 5, Unigraphics NX, and Enterprise Capital Costing. The Capital HarnessXC costs $18,200.
**Mentor Graphics, www.mentor.com**

## INTEGRATED CIRCUITS

### Buck converter powers FPGAs, ASICs, DSPs, microprocessors

With an input-voltage range of 2.4 to 5.5V and an output-voltage range as low as 0.6V, the EN5312Q1 buck converter features an integrated inductor that needs two low-cost ceramic capacitors. The 1A, 3W device incorporates voltage-mode control with a high switching frequency to provide a wide bandwidth-control loop, which enables transient performance with high-noise immunity. A three-pin VID programs the output voltage with a typical output ripple of 5 mV p-p. Users can choose one of seven preprogrammed output voltages or employ an external resistor divider. Output capacitance ranges from 10 to 60 µF without the need for external compensation adjustment. Available in a 5×4×1.1-mm QFN package and able to operate at speeds as high as 5 MHz, the EN5312Q1 costs $1.41 (1000).
**Enpirion, www.enpirion.com**

### Spectrum analyzer covers all Wi-Fi frequencies

Featuring a 2.4- to 6-GHz log-periodic directional antenna and 2.4- and 5-GHz omnidirectional antennas, the Wireless Wizard handheld spectrum analyzer includes power adapters, software to download data to a PC, and coverage of the 18-channel, 4.94- to 4.99-GHz public-safety band. The device stores antenna factors for all antennas, so users can make measurements in field strength (decibels referred to microvolts per meter). The Wireless Wizard costs $2950.
**Bantam Instruments, www.bantaminstruments.com**

### Storage-processor family uses eSATA cascading

Delivering power using advanced RAID (redundant-array-of-independent-disks) functions and Safe 33 and Safe 50 modes, the SteelVine storage-processor family targets home and SOHO (small-office/home-office) applications. Features include USB 2.0 host interfaces, advanced data protection with drive locking, single-button backup, and eSATA (external Serial Advanced Technology Attachment) cascading. Now available for sampling, the SteelVine family of processors will be available in January 2007 and will cost $5.
**Silicon Image, www.siliconimage.com**

### LDO regulators feature a quiescent current of 120 µA

These low-output-voltage, high-output-current LDO (low-dropout) regulators support output currents as high as 1.5A. With input voltages of 2.3 to 6V and output voltages of 0.8 to 5V, the LDO regulators have a full-current dropout voltage of 330 µV. The ceramic-output-capacitor-stable devices include power-good and shutdown functions. Applications for the regulators include high-performance embedded processors, controllers, and next-generation logic cores. The MCP1827 devices come in five-pin DDPAK and TO-220 packages. They are available in fixed- and adjustable-output-voltage versions selling for $1.09 and $1.17 (10,000), respectively. Available in three-pin DDPAK and TO-220 packages, the MCP1827S costs $1 (10,000).
**Microchip Technology Inc, www.microchip.com**

### Highly integrated motor-control chip has all necessary power FETs

Integrating all necessary power FETs, the L7208 hard-disk-drive motor-controller chip suits 1.8-in. and smaller consumer-equipment drives. The device uses Smooth Drive, the pseudosinusoidal digital-drive technique, minimizing acoustic noise from the spindle motor and suiting applications requiring quiet operation. The device also has a free-fall-sensor interface. Additional features include a Class AB output stage with zero deadband and minimal crossover distortion, power FETs delivering 0.5A peak current, and a voice-coil section including a 14-bit DAC. This register-controlled chip connects to the host system through a serial bus running at 50 MHz. Available in an LGA package, the L7208 motor controller costs $15.
**STMicroelectronics, www.st.com**

# productroundup

## INTEGRATED CIRCUITS

### Low-power audio codecs feature 7-mW playback

The PCM3793 and PCM3794 audio codecs feature a notch filter with programmable center frequencies, tone control, and 3-D enhancement. The PCM3793 drives 700 mW of output power per channel into an 8Ω load. The PCM3794 has no speaker outputs, allowing manufacturers to use an external amplifier. Both devices feature a 93-dB SNR and come in standard 32-pin, 5×5-mm$^2$ QFN packages. An available turnkey evaluation module includes a PC-based interface for programming the devices. The units sell for $4.50 and $4.25 (1000), respectively.

**Texas Instruments, www.ti.com**

### Receiver and transmitter support HDTVs

Joining the VastLane product family, the HDMI 1.3 SiI 9133 receiver and SiI 9134 transmitter semiconductors feature deep-color support for next-generation HDTVs. Suiting Blu-ray-disc and HD-DVD players in their highest resolutions, the deep-color feature allows the display of billions rather than millions of colors, the elimination of on-screen color banding, an increased contrast ratio, and the ability to represent more shades of gray. The semiconductors also support 30- and 36-bit color depths at 4:4:4 RGB or YCbCr and the 24-bit color depths that current HDTVs display. A boost in bandwidth from 4.95 to 6.75 Gbps allows support for resolutions of 720p and 1080i at 120 Hz, 36-bit-per-pixel color depth, and 12-bit video with 14-bit internal processing for improved accuracy. The 9134 transmits lossless compressed digital-audio formats supported in HDMI 1.3, including Dolby TrueHD and DTS-HD Master Audio. Available in a BGA-404 package, the SiI 9133 dual-input receiver costs $9.70 (10,000); the SiI 9134 transmitter is available in a TQFP-100 package and costs $5.25 (10,000).

**Silicon Image, www.siliconimage.com**

### Octal ADCs have a 70-dB SNR to Nyquist

Available in 9×9-mm, 64-pin LFCSPs, this series of octal ADCs targets use in portable medical devices and ultrasound machines. The 10-bit AD9212 and 12-bit AD9222, which consume less than 100 mW per channel, and the 14-bit, high-speed AD9252 feature 70-dB SNR to Nyquist. The 40M-sample/sec AD9212 and AD9222 cost $32 and $44 (1000), respectively. The 50M-sample/sec AD9212, AD9222, and AD9252 devices cost $40, $49, and $54 (1000), respectively.

**Analog Devices Inc, www.analog.com**

### Video crosspoint delivers black-level accuracy

Featuring security-camera switching and RGB and HDTV routing, the 300-MHz video crosspoint has a 6-MHz signal crosstalk of −90 dB and a single 5V supply operation. The device integrates dc-restore clamps, which users can disable. The clamps bias composite NTSC and PAL video by automatically adjusting the dc level of the most negative portion of the video to the reference voltage. The device also features a broadcast mode in which any single input can simultaneously transmit to all outputs. The 150-MHz broadcast mode suits keyboard, video, and mouse applications. The nonblocking 16 video inputs and 16 video outputs allow routing from any input signals to any output signals. You can individually program outputs to gains of one or two. Available in a 356-lead BGA package, the ISL59530 costs $45 (1000).

**Intersil, www.intersil.com**

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**EDN BUSINESS STAFF**

**PRESIDENT, BOSTON DIVISION**
Stephen Moylan, smoylan@reedbusiness.com; 1-781-734-8431; fax: 1-781-290-3431

**PUBLISHER, EDN WORLDWIDE**
John Schirmer, jschirmer@reedbusiness.com; 1-408-345-4402; fax: 1-408-345-4400

**OFFICE MANAGER**
Rose Murphy, MurphyS@reedbusiness.com; 1-781-734-8457; fax: 1-781-290-3457

**NORTHERN CA/SILICON VALLEY**
Patti Sellman
patti.sellman@reedbusiness.com
1-408-345-4439
fax: 1-408-345-4400

**PACIFIC NORTHWEST/NORTHERN CA/ID/NV/OR/WA/WESTERN CANADA**
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Roger Buckley, rbuckley@reedbusiness.com
1-972-216-5104, fax: 1-972-216-5105

**NATIONAL SALES DIRECTOR**
Alan Robinson
aarobinson@reedbusiness.com
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nmcdermott@reedbusiness.com
1-781-734-8130
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fax: +44 208-652-8249

**UK/NORWAY/SWEDEN/DENMARK/FINLAND/NETHERLANDS/BELGIUM/LUXEMBOURG**
John Waddell, jwadds@compuserve.com
+44 208-312-4696, fax: +44 208-312-1078

**AUSTRIA/GERMANY**
Adela Ploner, adela@ploner.de
+49 8131 366 99 20
fax: +49 8131 366 99 29

**ISRAEL**
Asa Talbar, talbar@inter.net.il
+972-3-5629565, fax: +972-3-5629567

**ITALY**
Roberto Laureri, media@laureriassociates.it
+39 02-236-2500, fax: +39 02-236-4411

**SWITZERLAND**
Gino Baretella, baretella@exportwerbung.ch
+41 1880-3545, fax: +41 1880-3546

**FRANCE/PORTUGAL/SPAIN**
Alain Faure, Alain.Faure@wanadoo.fr
+01 53 21 88 03, fax: +01 53 21 88 01

**JAPAN**
Toshiyuki Uematsu, t.uematsu@reedbusiness.jp
+81 3-5775-6057

**SOUTH KOREA**
Andy Kim, andy.kim@rbi-asia.com
+822 6363 3038, fax: +822 6363 3034

**SINGAPORE, MALAYSIA, THAILAND**
Chen Wai Chun, waichun.chen@rbi-asia.com
+65 6780 4533, fax: +65 6787 5550

**TAIWAN**
Charles Yang
+886 4 2322 3633, fax: +886 4 2322 3646

**AUSTRALIA**
David Kelly, david.kelly@rbi.com.au
+61 2-9422-2630, fax: +61 2-9422-8657

**HONG KONG**
Simon Lee, simonlee@rbi-asia.com.hk
+852 2965-1526
Dolf Chow, dolfchow@rbi-asia.com.hk
+852 2965-1531

**MARKETING COORDINATOR, EDN WORLDWIDE**
Tara Wietecha, tara.wietecha@reedbusiness.com
1-781-734-8450

**DIRECTOR OF CUSTOM PUBLISHING**
Cindy Fitzpatrick, cfitzpatrick@reedbusiness.com
1-781-734-8438, fax: 1-781-290-3438

**EDITORIAL/WEB PRODUCTION MANAGER**
Diane Malone, dmalone@reedbusiness.com
1-781-734-8445, fax: 1-781-290-3448

**ADMINISTRATION**
John Blanchard, Vice President of Manufacturing
Norm Graf, Creative Director
Gloria Middlebrooks, Graphic Production Director
Dorothy Buchholz, Group Production Director

**DESIGN**
Dan Guidera, Senior Art Director/Illustration

**RESEARCH DIRECTOR**
Rhonda McGee, rmcgee@reedbusiness.com
1-781-734-8264, fax: 1-781-290-3264

**CIRCULATION MANAGER**
Jeff Rovner, jrovner@reedbusiness.com
1-303-470-4477

**REED BUSINESS INFORMATION**
**Tad Smith**
Chief Executive Officer
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EDITED BY RON WILSON

# scope

CHART YOUR COURSE

## LOOKING AHEAD

### TO DESIGNCON 2007

**From its history as a Hewlett Packard proprietary show, to its stature today as a small but influential design conference, DesignCon, (www.designcon.com/2007), which will take place January 29 to February 1, continues to have things to offer along a number of engineering tracks. This year, keynote speakers will include Steve Polzin, senior fellow and chief platform architect at AMD; Wim Roelandts, president, chief executive officer, and chairman of Xilinx; and Leah Jamieson, dean of engineering at Purdue University. Technical papers will range from SystemC modeling of DRAM subsystems, to transmission-line measurements, to SOC (system-on-chip) design and packaging issues. A parallel set of business-forum presentations will examine strategic issues facing design teams.**

## LOOKING BACK

### Toward the beginnings of robotic vision

A miniature photocell accurately determines both direction and intensity of a light source. As many as four separate cells of conventional design may be replaced by one of these units. Developed by RCA, the device is based on a recently discovered phenomenon that occurs when light is focused by a lens on a semiconductor junction. If the light strikes the junction to either side of center, a small side-to-side voltage is generated. Termed lateral voltage, it is distinct from the known voltage generated across the junction from front to rear by light shining directly on the junction. … [This scenario permits] the cell to produce a signal which varies with the angle between the cell axis and the light direction. Simultaneously, another signal registers intensity.

—*Electrical Design News*, December 1956

## LOOKING AROUND

### At the Christmas selling season around the world

Granted that a visit to a mall in the United States right now is enough to induce agoraphobia in Dale Carnegie. But what's going on inside those crowded halls of retail commerce could set the fate of the electronics industry for the next year or two. Automotive applications continue to increase their semiconductor content, to the benefit mostly of a few large companies. Ditto for the server market, with a mostly different set of vendors. Similarly, an established infrastructure—mostly in Asia now—will be the beneficiary if Microsoft Vista is able to pump up PC sales. But the industry is pinning much of the growth it needs in 2007 and beyond on consumer products, from the bargain-priced MP-3 player, to the next feature phone, to the giant home-theater system. If retail sales are slow, the disappointment will not only further increase inventories, but also discourage new-product development and investment, with longer reaching impact.

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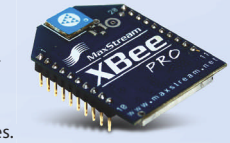

ZigBee/IEEE 802.15.4 compliant solution that delivers critical data between devices. Operates within the ISM 2.4GHz frequency band, 1mW power output up to 100m range, U.FL.RF connector, -40°C to 85°C temp. range with chip or wire options. Supports advanced networking and low-power modes.

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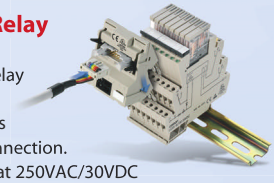
## G2RV Slim Relay



Industrial slim relay rated with large plug-in terminals for a reliable connection. Rated at full 6A at 250VAC/30VDC over 6,000 operations at 40°C. LED indicator, clear case, and mechanical flay allow easy and immediate visual operation verification. Slim outline to save space in high-volume rack and PLC applications.

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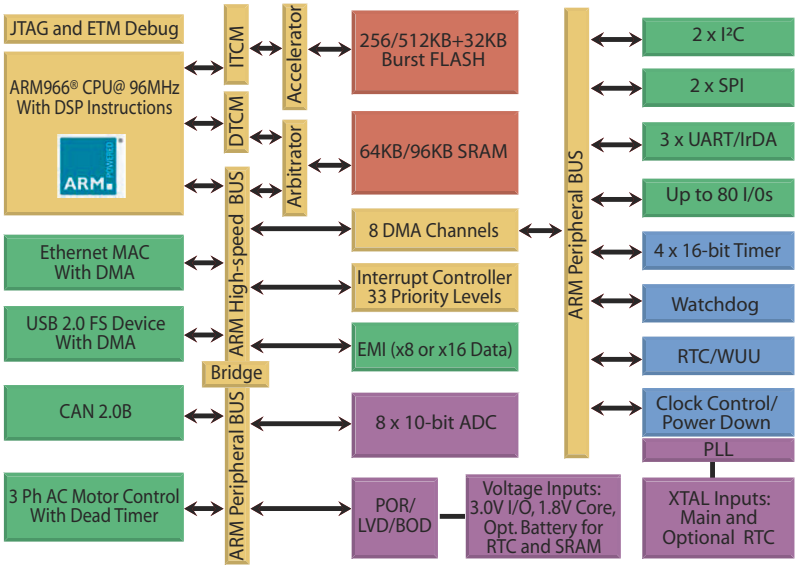


***World's first ARM9-based general-purpose Flash microcontroller enables new generation of networked embedded applications***


***It's All Inside:*** *STR9 MCUs minimize the need for external components and add innovative features on the inside such as a 1µA real-time clock and a full-function system supervisor.* ***Rapid Transit:*** *96MHz operation, optimized internal data and instruction paths, and 9 DMA channels ensure data moves where you want it, when you want it.* ***No Crowded Spaces:*** *Up to 96KB of SRAM and 544KB of Flash memory accommodate complex applications, TCP/IP, real-time operating systems and multinational products.*

| Part Number | Flash Memory (KB) | RAM (KB) | A/D Inputs | (IC/OC/ PWM) | Other | Serial Interface | GPIO (HI Current) | Package | Supply Voltage | Special Features |
|---|---|---|---|---|---|---|---|---|---|---|
| STR910FM32X | 256 + 32 | 64 | 8x10-bit | 7x16-bit (8,8,7) | RTC WDG | 2xSPI 2xI²C 3xUART w/IrDA | 40 (16) | LQFP80 | Core: 1.8V I/O: 2.7 to 3.6V | CAN |
| STR910FW32X | 256 + 32 | 64 | 8x10-bit | | | | 80 (16) | LQFP128 | | CAN, EMI |
| STR911FM42X | 256 + 32 | 96 | 8x10-bit | | | | 40 (16) | LQFP80 | | USB, CAN |
| STR911FM44X | 512 + 32 | 96 | 8x10-bit | | | | 40 (16) | LQFP80 | | USB, CAN |
| STR912FW42X | 256 + 32 | 96 | 8x10-bit | | | | 80 (16) | LQFP128 | | Ethernet, USB, CAN, EMI |
| STR912FW44X | 512 + 32 | 96 | 8x10-bit | | | | 80 (16) | LQFP128 | | Ethernet, USB, CAN, EMI |

**For further information, datasheets, and application notes, visit www.st.com/str9**

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